FACULTY PROFILE

Nanduri Samba murthy

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D.No:1-290, Near Ramakrishna theatre Road,
Gudlvalleru Engineering College, Gudlavalleru-521356.

Academic Qualifications

S. No	Name of the Degree *(Starting from Ph.D to 10th Class)*	University/College	Percentage of Marks/Grade	Specialization
1	Ph.D	JNTUK, KAKINADA	-	VLSI Design
2	M.TECH	GUDLVALLERU ENGG.COLLEGE, GUDLAVALLERU	79.5	Embedded systems
3.	B.TECH	JNTUH,HYD.	60.80	ECE
4.	DIPLOMA	A.A.N.M&V.V.R.S.R POLYTECHNIC, GUDLAVALLERU	71.40	ECE
5.	S.S.C	P.L.S. Z.P.HIGH SCHOOL,AKIVIDU	76.5%	-

Professional Experience

S. No	Designation	Institution Name	Working Period	
			From	To
1.	Lecturer	A.AN.M&VVRSR POLYTECHNIC Gudlavalleru.	2007	2013
2.	Assistant Professor	GUDLAVALLERU ENGG.COLLEGE	2013	Till Date

Professional Body Membership

S. No	Name of the Professional body	Membership Number
1.	The Institute of Engineers (India)	AM157511-5

Papers Published in Journals No. :03

1. M.Kamaraju, N.Sambamurthy, "FPGA Implementation of Multiprocessor Core Architecture for Embedded Concurrent Computing", IET digital library, DOI: 10.1049/Cp.2012.2491, ISBN: 978-1-84919-929-2.4, PP:75–80.

2. N.Sambamurthy, Sk.HasaneAhamad "Prevention of Train Accidents Using Wireless Sensor Networks" International Journal of Engineering Research and Applications, vol.03, issue.06, ISSN:2248-9622,Nov-Dec 2013,PP.1592-1597 (Impact factor:1.92).

3. N.Sambamurthy, M. Kamaraju, "Design and development of concurrent computing based multiprocessor architecture with Multi UART", in proc. of IEEE-EESCO-Jan 2015, coyright:978-1-4799-7678-2/15$ 2015,©IEEE.pp.445-454.

4. N.Sambamurthy, M. Kamaraju, "A Survey on Image visual Detection and Matching Techniques for Real-Time Environment" IET journal IECV SCI indexed journal – under Review process. (communicated).

5. N.Sambamurthy, M.Kamaraju,"FPGA Implementation of PSO Based RGB-Y Filter" International Journal of Advanced Trends in Computer Science and Engineering,volume-9, issue-4,2020.

6. N.Sambamurthy, M.Kamaraju," FPGA Based Optimized Reconfigurable Base-2 Constant Coefficient Multiplier Architecture for Image Filtering", International Journal of Engineering and Advanced Technology (IJEAT), volume-9,issue-4,2020,pp-822-825.

Papers Published in Conferences No. :01

1. M. Kamaraju, N.Sambamurthy, "FPGA Implementation of Multiprocessor Core Architecture with multichannel UART" NCIET-2014,PP. 265-269.
2. M. Kamaraju, N.Sambamurthy, "High Performance Image Feature Detection and Matching", NITW, Springer conference, 2020, PP.543-548.

Workshops Organized No. : 01

1. One day workshop on "ARM 7 programming and its applications" organized by department of ECE, Gudlavalleru Engineering College, Gudlavalleru on 9th July 2015

Workshops /Conferences /Seminars Attended No. : 07

1. one day seminar on "Engineering education and research" conducted by NI instruments, 19th July 2020.

2. one week workshop on "Advances in VLSI design" conducted by IIT Kharagpur during 2nd -6th January 2015.

3. One day workshop on "Research in Energy Management Wireless Networks & Smart Transportation Systems" organized by The Institute of Engineers (India), Vijayawada Local Centre, Vijayawada on 29th March 2015.

4. One day workshop on "Research & Development Facilitation" organized by The Institute of Engineers (India), Vijayawada Local Centre, Vijayawada on 29th March 2015.

5. One day workshop on "Speech Processing: Current Challenges and Hands-on Experience" organized by department of ECE, Gudlavalleru Engineering College, Gudlavalleru on 23rd August 2014.

6. Three day National Workshop on "Theory & Applications of Intelligent Signal Processing", organized by department of ECE, Gudlavalleru Engineering College, Gudlavalleru during 28th February to 2nd March 2014.

7. Two week ISTE workshop on "Signals & Systems" conducted by IIT Kharagpur in association with department of ECE, Gudlavalleru Engineering College, Gudlavalleru during 2nd -12th January 2014.

Certifications/Training Programs Attended No. :03

1. 15 days orientation program on "Research Methodology", organized by JNTUK, KAKINADA during 1st - 15th May 2015.

2. 15 days orientation program on "Intellectual property rights", organized by JNTUK, KAKINADA during 16th-30th May 2015.

3. Faculty Development Program on "VLSI and Embedded System Design" organized by department of ECE, Gudlavalleru Engineering College, Gudlavalleru during 7th – 8th July 2012.

4. Faculty Development Program on "Embedded System Design" organized by department of ECE, Gudlavalleru Engineering College, Gudlavalleru during 19th – 25th July 2020.

Guest Lectures Delivered No. :01

"Concurrent computing", for faculty at Gudlavalleru Engineering College, Gudlavalleru on 9th April 2014.

"Low power VLSI techniques", for faculty at Gudlavalleru Engineering College, Gudlavalleru on 27th septemer2016.

Subjects Handled

Under Graduation

- Electronics measurements and instrumentation
- Microprocessor and microcontrollers
- Computer networks
- Microprocessors and Multicore systems
- Microprocessors and interfacing

Post Graduation

- Embedded system design
- Sensors and actuators
- Embedded systems lab
- HDL Simulation lab

Laboratories Handled

Under Graduation

- Microprocessor and microcontrollers Lab
- Microprocessors and interfacing Lab

Post Graduation

- Embedded systems lab
- HDL Simulation lab

Other Responsibilities

College Level

1. Disciplinary committee at the time of GEC FEST-2013, 2014,2015,2016,2017.

Department Level

1. Internal examinations co-ordinator for the year 2014-2017.

Projects Guided:

Under Graduation

S. No	Name of the project	Year
1.	FPGA implementation of automatic tollgate systems	2013
2.	Microcontroller based traffic guidance system	2014
3.	FPGA implementation of self timed adder	2015
4.	FPGA implementation of low power RISC Processor	2016.
5.	FPGA implementation of self configured timer	2017
6	FPGA implementation of median filter	2018
7.	Design of self parity checker	2019
8.	FPGA implementation of low power median filter	2020

Post Graduation

S.No	Name of the project	Year

1.	Prevention of train accidents using wireless sensor networks	2013
2.	Design and analysis of AES encryption and decryption	2014
3.	Power optimized CODEC	2015
4.	Design and analysis of logic-in-memory based multiprocessor architecture for multi data transfer schemes	2016

Books Published No. :01

1.**N.SAMBMURTHY,** Titled by **"COMMUNICATION ENGINEERING",** For Polytechnic ECE Students Published by FALCON publishers, Hyderabad during 2012

R&D and Consultancy:

S. No	Project Title	Source of Funding	Duration	Role	Status
1.	A Novel Automotive Vehicle Smart Parking, Tracking and Toll collection System with Computational Intelligence Based SoC using IoT.	Science and Engineering Res earch Board (SERB)	3-years	Co-investigator	Communicated (Under Review Process)
2.	Design of novel digital auto starter	UBA	1-year	Prinicipal investigator	accepted

DETAILS OF PROJECT WORK:

Project #1:

Title : PC BASED TWO CHANNEL OSCILLOSCOPE. –----*DIPLOMA*

Hardware: 1. Microcontroller (AT 89c51).

2. RS-232.

3. PC.

Project #2:

Title : VHDL IMPLEMENTATION OF ETHERNET CSMA/CD PROTOCOL --*B.Tech*

Software: MODELSIM, XILINX.

Project #3:

Title : FPGA IMPLEMENTATION OF MULTIPROCESSOR CORE ARCHITECTURE FOR EMBEDDED CONCURRENT COMPUTING. ---*M.Tech*

Software: MODELSIM, XILINX.

Research work: Ph.D.(Pre Ph.D Completed)

Research Topic : Design and Development of Embedded SoC architecture design for Real time Environment.

Tools: Matlab,Xilinx and FPGA Hardware.

Curriculum Design and Development

1. Embedded System Lab
2. Embedded system design
3. Sensors and actuators

Academic Rewards / Achievements: NIL

1.
2.
3.

Extra Curricular Activities

1.Acted as BoS member for department of ECE, Gudlavalleru Engineering College, Gudlavalleru on 2nd August 2014 , 25th May 2015 and 1st March 2017.

2. Acted as BoS member for department of ECE, Gudlavalleru Engineering College, Gudlavalleru on 2nd August 2014 , 25th May 2019 and 1st March 2020.

Declaration

I hereby declare that all the above-furnished information is correct to the best of my knowledge.

Date: 29/09/2020 Signature

Place: Gudlavalleru (N.SAMBAMURTHY)