ACADEMIC REGULATIONS
COURSE STRUCTURE
AND
DETAILED SYLLABUS

EMBEDDED SYSTEMS

Department of Electronics & Communication Engineering

M.Tech Two Year Degree Course

(Applicable for the batch admitted from 2014-15)

GUDLAVALLERU ENGINEERING COLLEGE

(An Autonomous Institute with Permanent Affiliation to JNTUK, Kakinada)

Seshadri Rao Knowledge Village

GUDLAVALLERU - 521 356, Krishna District, Andhra Pradesh

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ACADEMIC REGULATIONS

M.Tech - Embedded Systems

ACADEMIC REGULATIONS

1. Duration of the Program

The duration of the program is two academic years consisting of four semesters. However, a student is permitted to complete the course work of M.Tech program in the stipulated time frame of **FOUR** years from the date of joining.

2. Minimum Instruction Days

Each semester consists of a minimum of ninety instruction days.

3. Program Credits

Each specialization of the M.Tech programs is designed to have a total of 80 credits and the student shall have to complete the two year course work and earn all the 80 credits for the award of M.Tech Degree.

4. Attendance Regulations

4.1 A student shall be eligible to appear for End Semester Examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.

4.2 Condoning of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester will be considered for genuine reasons such as medical grounds and participation in co-curricular and extra-curricular activities and shall be granted only after approval by a committee duly appointed by the college. Student should submit application for medical leave along with medical certificate from a registered medical practitioner within three days from reporting to the class work after the expiry of the medical leave. In case of participation in co-curricular and extra-curricular activities, either in the college or other colleges, students must take prior written permission from HoD concerned and should also submit the certificate of participation from the organizer of the event within three days after the completion of the event. Only such cases will be considered for condoning attendance shortage.

4.3 A student shall be eligible to claim for condonation of attendance shortage only once during the two years (four semesters) course work.

4.4 A student will not be promoted to the next semester unless he satisfies the attendance requirement of the current semester. He may seek re-admission for that semester when offered next.

4.5 Shortage of Attendance below 65% in aggregate shall in *NO* case be condoned.

4.6 Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examination of that semester and their registration shall stand cancelled.

4.7 A fee stipulated by the college shall be payable towards condoning attendance shortage.

5. Examinations and Scheme of Evaluation

5.1 Theory Courses:

Each theory course shall be evaluated for a total of 100 marks, consisting of 40 marks for internal assessment and 60 marks for semester end examination.

***Internal Assessment*:**

i) Out of 40 marks for internal assessment, 20 marks are for continuous assessment in the form of assignment and seminar and 20 marks are based on two mid-term examinations.

ii) Of the 20 marks for continuous assessment, 10 marks each for assignment and seminar.

iii) Each mid-term examination is conducted for 40 marks with two hours duration. Each mid-term examination consists of four questions, each for 10 marks. All the questions need to be answered.

iv) Sum of the 75% marks of best scored mid-term examination and 25% marks of other mid-term examination are scaled down for 20 marks.

***External Assessment*:**

Semester End Examination will have 8 questions, each for 12 marks, out of which 5 questions are to be answered.

5.2 Laboratory Course:

i) For practical subjects the distribution shall be 40 marks for Internal Evaluation and 60 marks for the End-Examinations. There shall be continuous evaluation by the internal subject teacher during the semester for 40 internal marks. Of the 40 marks for internal, 30 marks shall be for day-to-day performance (20 marks for day-to-day evaluation and 10 marks for Record) and 10 marks for an internal laboratory test conducted towards the end of semester.

ii) Semester End examination shall be conducted by the teacher concerned and external examiner for 60 marks.

5.3 Seminar:

For seminar, a student under the supervision of a faculty member, shall collect the literature on an advanced topic related to his specialization and critically review the literature and submit it to the department in a report form two weeks before the end of the 3rd semester and shall make an oral presentation before the Departmental Review Committee consisting of the supervisor and a senior faculty member / Head of the Department. There

shall be an internal evaluation for 50 marks in the form of viva-voce examination and assessment of report and its presentation. There will be NO external evaluation.

If a candidate fails to secure the minimum marks prescribed for successful completion, he has to re-register by paying the prescribed fee at the beginning of 4th semester or subsequent semesters. He has to submit a fresh report two weeks before the end of that semester and appear for the evaluation by the committee.

5.4 Comprehensive Viva-Voce:

Comprehensive Viva-Voce examination is conducted for 50 marks at the end of third semester in all the subjects of first two semesters of the course by a committee consisting of two senior faculty members of the department. There will be NO external evaluation.

If a candidate fails to secure the minimum marks prescribed for successful completion, he has to re-register by paying the prescribed fee at the beginning of 4th semester or subsequent semesters and undergo Viva-Voce examination towards the end of that semester.

5.5 Project Work:

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

i) A Project Review Committee (PRC) shall be constituted for each specialization with Head of the Department as Chairman and two other senior faculty members.

ii) Registration of Project Work: A candidate who has been promoted to 3rd semester shall be eligible to register for the project work.

iii) The eligible candidate can choose his project supervisor and submit the title, objective, abstract and plan of action of the proposed project work to the department for approval by the PRC. The candidate whose proposal is approved by the PRC shall register for the project work. The minimum duration of project work will be 36 weeks from the date of registration.

iv) If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. In case of such changes, the candidate has to register afresh.

v) There shall be three reviews on the progress of the project work by the PRC with an interval of 12 weeks. The candidate needs to submit a report on the progress of his work and present it before the PRC for assessment. The PRC may suggest for an extension of date of submission of dissertation if the progress of work is not satisfactory or absent himself for the review.

vi) A candidate who has passed all the theory, laboratory, seminar and comprehensive viva-voce examinations and shown satisfactory progress of project work is permitted to submit the dissertation after 36 weeks from the date of registration.

vii) If a candidate fails to submit the dissertation by the end of the 4th semester, he has to take the permission for an extension by paying the semester(s) tuition fee.

viii) Three copies of the Project Thesis certified by the supervisor shall be submitted to the Department.

ix) Project evaluation and Viva-Voce examination is conducted at the end of 4th semester by a committee consisting of Project Supervisor, senior faculty of the department, HoD and an External Examiner nominated by the Chief Controller of Examinations out of a panel of three examiners suggested by the department.

The following grades are awarded for the project work:

i. Excellent
ii. Very Good
iii Good
iv. Satisfactory
v. Unsatisfactory

The Grade "unsatisfactory" is treated as Fail. Failed Students should take supplementary examination after making required modifications, if any, in the dissertation with a minimum gap of 8 weeks by paying the required examination fee.

6. Criteria for Passing a Course and Award of Grades:

6.1 Criteria for Passing a Course:

i) A candidate shall be declared to have passed in individual theory/ drawing / design course / laboratory if he secures a minimum of 50% aggregate marks (internal & semester end examination marks put together), subject to securing a minimum of 40% marks in the semester end examination.

ii) The candidate shall be declared to have passed in seminar / comprehensive viva-voce if he secures 50% marks.

iii) The candidate shall be declared to have successfully completed the project work if he secures a minimum of 'satisfactory' grade in the project evaluation and viva-voce examination.

iv) On passing a course of a program, the student shall earn assigned credits in that course.

6.2 Method of Awarding Letter Grade and Grade Points for a Course:

A letter grade and grade points will be awarded to a student in each course based on his performance, as per the grading system given below.

Theory Course (%)	Laboratory (%)	Grade Points	Letter Grade
³ 90	³ 90	10	S
³ 80 & < 90	³ 80 & < 90	9	A
³ 70 & < 80	³ 70 & < 80	8	B
³ 60 & < 70	³ 60 & < 70	7	C
³ 50 & < 60	³ 50 & < 60	6	D
< 50	< 50	0	F (Fail)

S : Outstanding **A** : Excellent **B** : Very Good
C : Good **D** : Fair

6.3 Calculation of Semester Grade Point Average (SGPA)* for semester:

The performance of each student at the end of the each semester is indicated in terms of SGPA. The SGPA is calculated as given below:

SGPA = $\frac{\sum(CR \times GP)}{\sum CR}$ for each semester.

where CR = Credits of a course
GP = Grade Points awarded for a course

* SGPA is calculated for a candidate who passed all the courses in that semester.

6.4 Eligibility for Award of M.Tech Degree:

A student will be declared eligible for the award of the M.Tech Degree if he fulfills the following academic regulations.

(a) Pursued a course of study for not less than two academic years and not more than four academic years.

(b) Registered for **80** credits and secured all **80** credits.

(c) Students, who fail to complete their Two years Course of study within Four years or fail to acquire the **80** Credits for the award of the degree within four academic years from the year of their admission shall forfeit their seat in M.Tech course and their admission shall stand cancelled.

6.5 Calculation of Cumulative Grade Point Average (CGPA)* for Entire Program:

The CGPA is calculated as given below:

CGPA = $\frac{\sum(CR \times GP)}{\sum CR}$ for entire program.

where CR = Credits of a course
GP = Grade points awarded for a course

* CGPA is calculated for a candidate who passed all the prescribed courses excluding project work.

6.6 Award of Division:

After satisfying the requirements prescribed for the completion of the program, the student shall be eligible for the award of M.Tech Degree and shall be placed in one of the following grades:

CGPA	Class	Letter Grade	Description
³ 7.5	First Class with Distinction	A	Excellent
³ 6.5 & < 7.5	First Class	B	Good
³ 6.0 & < 6.5	Second Class	C	Fair

7. Supplementary Examinations :

i) Supplementary examinations will be conducted once in a year along with regular examinations.

ii) Semester end supplementary examinations shall be conducted till next regulation comes into force for that semester after the conduct of the last set of regular examinations under the present regulation.

iii) Thereafter supplementary examinations will be conducted in the equivalent courses as decided by the Board of Studies concerned.

8. Readmission Criteria :

A candidate, who is detained in a semester due to lack of attendance has to obtain written permission from the Principal for readmission into the same semester after duly fulfilling the required norms stipulated by the college and by paying the required tuition fee and special fee in addition to paying an administrative fee of Rs. 1,000/-.

9. Break in Study :

Student, who discontinues the studies for what-so-ever reason, can get readmission into appropriate semester of M.Tech program only with the prior permission of the Principal of the College, provided such candidate shall follow the transitory regulations applicable to the batch he joins. An administrative fee of Rs.2,000/- per each year of break in study, in addition to the prescribed tuition and special fees should be paid by the candidate to condone his break in study.

10. Transitory Regulations:

A candidate, who is detained or discontinued in a semester, on readmission shall be required to do all the courses in the curriculum prescribed for the batch of students in which the student joins subsequently. However, exemption will be given to those candidates who have already passed such courses in the earlier semester(s) he was originally admitted into and he will be offered

substitute subjects in place of them as decided by the Board of Studies. However, the decision of the Board of Studies will be final.

10.1 A student who is following JNTUK curriculum and detained due to shortage of attendance at the end of the first semester of first year shall join the autonomous batch of first year first semester. Such students shall study all the courses prescribed for the batch in which the student joins and considered on par with regular candidates of Autonomous stream and will be governed by the autonomous regulations.

10.2 A student who is following JNTUK curriculum, detained due to shortage of attendance at the end of the second semester of first year shall join with the autonomous batch in the second semester. Such candidates shall be required to pass in all the courses in the program prescribed by the Board of Studies concerned for that batch of students from that semester onwards to be eligible for the award of degree. However, exemption will be given in the courses of the semester(s) of the batch which he had passed earlier and substitute subjects are offered in place of them as decided by the Board of Studies. The student has to clear all his backlog subjects of first semester by appearing for the supplementary examinations conducted by JNTUK for the award of degree. The total number of credits to be secured for the award of the degree will be sum of the credits of first semester under JNTUK regulations and the credits prescribed in second semester in which a candidate seeks readmission and subsequent semesters under the autonomous stream. The class will be awarded based on the academic performance of a student in the autonomous pattern.

11. Withholding of Results

If the student has not paid the dues, if any, to the College or if any case of indiscipline is pending against him, his examinations results and degree will be withheld.

12. Malpractices :

i) The Principal shall refer the cases of malpractices in internal assessment tests and semester end examinations to a malpractice enquiry committee constituted by him for the purpose. Such committee shall follow the approved levels of punishment. The Principal shall take necessary action against the erring students based on the recommendations of the committee.

ii) Any action by the candidate trying to get undue advantage in the performance or trying to help another, or derive the same through unfair means is punishable according to the provisions contained hereunder.

DISCIPLINARY ACTION FOR MALPRACTICES/IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices / Improper conduct	Punishment
If the candidate		
1.a	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers, cameras, bluetooth devices etc. or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination.)	Expulsion from the examination hall and cancellation of the performance in that subject only.
b	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through Cell phones with any candidates or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The hall ticket of the candidate shall be cancelled.

3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for the examinations of the remaining subjects of that semester. The candidate is also debarred for two consecutive semesters from class work and all university examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the impostor is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles the Answer book or takes out or arranges to send out the question paper during the examination or answer book during or after the examination.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The candidate is also debarred for two consecutive semesters from class work and all university examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.

5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/ Assistant Chief Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in or around the examination hall or organises a walkout or instigates others to walkout or threatens the officer-in-charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the Officer-in-charge or any person on duty in or outside the examination hall of any of his relations or indulges in any other act of misconduct or mischief which results in damage to or destruction of property in the examination hall or any part of the college campus or engages in any other act which in the opinion of the Officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The candidate is also debarred for two consecutive semesters from class work and all university examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.

8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The candidate is also debarred and forfeits the seat.
9	If student of the college who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clauses 6 to 8.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the college will be handed over to the police and a police case is registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester examinations.

12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be referred to the Chief Superintendent of Examinations for future action towards suitable punishment.

iii) The involvement of the staff, who are in charge of conducting examinations, valuing examination papers and preparing / keeping records of documents related to the examinations in such acts (inclusive of providing incorrect or misleading information) that infringe upon the course of natural justice to one and all concerned at the examination shall be viewed seriously and appropriate disciplinary action will be taken after thorough enquiry.

13. Other Matters

i) Physically challenged candidates who have availed additional examination time and a scribe during their BE/B.Tech examinations will be given similar concessions on production of relevant proof/documents. Students who are suffering from contagious diseases are not allowed to appear either for internal or semester end examinations.

ii) The students who participated in coaching / tournaments held at State / National / International levels through University / Indian Olympic Association during semester end external examination period will be promoted to subsequent semesters as per the guidelines of University Grants Commission Letter No. F.1-5/88 (SPE/PES), dated 18-08-1994.

iii) The Principal shall deal in an appropriate manner with any academic problem which is not covered under these rules and regulations, in consultation with the Heads of the Departments and subsequently such actions shall be placed before the Academic Council for ratification. Any emergency modification of regulation, approved in the meetings of the Heads of the Departments shall be reported to the Academic Council for ratification.

14. General

i) The Academic Council may, from time to time, revise, amend or change the regulations, schemes of examination and /or syllabi.

ii) The academic regulations should be read as a whole for the purpose of any interpretation.

iii) In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman of the Academic Council is final.

iv) Wherever the word he, him or his occurs, it will also include she, her and hers.

COURSE STRUCTURE

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SYLLABUS

M.Tech - Embedded Systems

COURSE STRUCTURE

I Semester

Sl. No.	Name of the Course / Laboratory	No.of Periods per week		No.of Credits
		L	P	
1	Embedded Systems Design	4	-	3
2	VLSI Technology and Design	4	-	3
3	Advanced Digital Signal Processing	4	-	3
4	Embedded - C	4	-	3
5	Elective - I	4	-	3
6	Elective - II	4	-	3
7	Hardware Description Language Lab	-	6	3
	Total	**24**	**6**	**21**

II Semester

Sl. No.	Name of the Course / Laboratory	No.of Periods per week		No.of Credits
		L	P	
1	CMOS Analog and Digital Design	4	-	3
2	Digital Signal Processors and Architecture	4	-	3
3	Embedded Computing	4	-	3
4	Wireless Sensor Networks	4	-	3
5	Elective - III	4	-	3
6	Elective - IV	4	-	3
7	Embedded Systems Lab	-	6	3
	Total	**24**	**6**	**21**

III Semester

Sl. No.	Name of the Course / Laboratory	No.of Credits
1	Seminar	2
2	Comprehensive Viva-Voce	2
3	Dissertation (Initiated in third semester)	-
	Total	**4**

IV Semester

Sl. No.	Name of the Course / Laboratory	No.of Credits
1	Dissertation (Carried out in third & fourth semesters)	34
	Total	**34**

Electives:

I Semester	II Semester
Elective - I	**Elective - III**
Principles of Digital System Design	Sensors and Actuators
Embedded Real Time Operating Systems	System on Chip Design
ARM Architecure and Programming	Design of Fault Tolerant Systems
Elective - II	**Elective - IV**
Embedded Software Concepts	Micro Electro Mechanical Systems
Advanced Computer Architecure	Embedded Networking
Hardware Software Co-Design	CPLD and FPGA Architectures

SYLLABUS

EMBEDDED SYSTEMS DESIGN

I - Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To gain knowledge on basic quantitative principles of embedded system design.
- To study about embedded firmware development concepts.

Learning Outcomes:

Students will be able to

- understand embedded system concepts.
- interface I/O devices with core of the system.
- apply the OS concepts to develop embedded system.

UNIT - I: Introduction

Definition of embedded system, embedded systems Vs general computing systems, history of embedded systems, processor and memory organization – structural units in a processor, software embedded into a system, ISA architecture models, internal processor design, processor selection for an embedded system, processor performance.

UNIT - II: Memory and Device Drivers

Board memory – ROM, RAM, auxiliary memory, memory management of external memory, performance; Device drivers-device drivers for interrupt-handling, memory, on-board bus and board I/O.

UNIT - III: Interfacing I/O

Embedded board input/output – serial versus Parallel I/O, interfacing the I/O components, I/O components and performance; board buses – bus arbitration and timing, integrating the bus with other board components, bus performance.

UNIT - IV: Operating Systems

Embedded operating systems – multitasking and process management; OS standards example – POSIX, OS performance guidelines.

UNIT - V: Design and Development

Embedded system design and development lifecycle model, creating an embedded system architecture, embedded software development process and tools-translational tools, debugging tools, testing on host machine, simulators, laboratory tools, linking and locating software, issues in hardware-software design and co-design.

Text Books:

1. Tammy Noergaard “Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers”, Elsevier (Singapore) Pvt.Ltd.Publications, 2005. (Units: II to V)
2. Rajkamal, “Embedded Systems: Architecture, Programming and Design”, TMH Publications, Second Edition,2008. (Units: I, V)

Reference Books:

1. Frank Vahid, Tony Givargis, “Embedded System Design”, John Wiley.
2. Lyla, “Embedded Systems”, Pearson, 2013.
3. David E. Simon, “An Embedded Software Primer”, Pearson Education.

VLSI TECHNOLOGY AND DESIGN

I – Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Pre-requisites:

- A strong background in circuits, familiarity with simple MOS models and basic understanding of logic design, engineering sciences is required.

Course Objectives:

- To introduce the fabrication process of MOS devices.
- To familiarize with electrical properties, performance estimation, design rules and layouts.
- To familiarize with various methods of floor planning and layout synthesis.

Learning Outcomes:

Students will be able to

- understand different IC fabrication technologies.
- realize CMOS circuits.
- apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnects.
- apply the floor planning and chip design techniques for a specific digital system.

UNIT - I: Introduction to MOS Technologies

Introduction, planar process technology steps, NMOS fabrication, CMOS fabrication, BiCMOSand SOI technology.

UNIT - II: Basic Electrical Properties of MOS, CMOS and BiCMOS Circuits

Basic MOS transistors, I_{ds}-V_{ds} relationships, threshold voltage V_t, g_m, g_{ds} and ω_0, pass transistor, MOS, CMOS and BiCMOS inverters, Z_{pu}/Z_{pd} for cascaded inverters, MOS transistor circuit model, latch-up in CMOS circuits.

UNIT - III: Logic gates and Performance Estimation

Static complementary gates, switch logic, alternative gate circuits, scaling, resistance estimation, capacitance estimation, inductance, switching characteristics, transistor sizing, charge sharing, low power gates, resistive and inductive interconnect delays.

UNIT - IV: Combinational and Sequential Logic Networks

Layouts, simulation, network delay, interconnect design, power optimization, switch logic networks, gate and network testing, memory cells and arrays, clocking disciplines, power optimization, design validation and testing.

UNIT - V: Floor Planning and Chip Design

Floor planning methods, off-chip connections, high-level synthesis, architecture for low power, SoCs and embedded CPUs, architecture testing, layout synthesis and analysis, scheduling and printing; hardware/software co-design, chip design methodologies- a simple design example.

Text Books:

1. K. Eshraghian. D, A.Pucknell, “Essentials of VLSI Circuits and Systems”, PHI of India Ltd,3rd Edition, 2005. (Units: I, II)
2. Wayne Wolf, “Modern VLSI Design”, Pearson Education, fifth India Reprint, 3rd Edition, 2005. (Units: I, III, IV, V)

Reference Books:

1. N.H.E Weste, K.Eshraghian, “Principles of CMOS Design”, Adison Wesley, 2ndEdition.
2. Fabricius, “Introduction to VLSI Design”, MGH International Edition, 1990.
3. Baker, Li Boyce, “CMOS Circuit Design, Layout and Simulation”, PHI, 2004.

ADVANCED DIGITAL SIGNAL PROCESSING

I – Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To explore the concepts and applications of multi-rate signal processing.
- To learn concepts of signal processing in power spectrum estimation and variable filters.

Learning Outcomes:

Students will be able to

- design and implement multi-rate systems.
- perform forward and backward predictions, noise cancellation using different techniques.
- design LMS and RLS adaptive filters.
- understand different spectral estimation techniques and linear prediction.

UNIT - I: Multirate Signal Processing and Applications

Up and down sampler, decimation, interpolation, sampling rate conversion, multistage sampling rate conversion, poly-phase structures for decimator and interpolator, filter bank implementation: two-channel filter banks, QMF filter banks

UNIT - II: Linear Estimation and Prediction

Linear prediction- forward and backward predictions, solutions of the normal equations- Levinson- Durbin algorithms; least mean squared error criterion - Wiener filter for filtering and prediction, FIR and IIR wiener filters.

UNIT - III: Adaptive Filters

Applications of adaptive filters, adaptive direct form FIR filters using LMS and RLS algorithms, adaptive lattice-ladder filters.

UNIT - IV: Power Spectral Estimation

Estimation of spectra from finite duration of a signal –The periodogram-use of DFT in power spectral estimation –non-parametric methods for power spectrum estimation – Bartlett, Welch and Blackman–Tukey methods –comparison of performance of non – parametric power spectrum.

UNIT - V: Parametric Power Spectrum

Estimation methods: Parametric methods - relationship between auto correlation and model parameters, AR, MA, ARMA models for power spectral estimation, yule-walker and burg methods for AR model parameters.

Text Books:

1. G. John Proakis and G. Dimitris Manolakis, “Digital Signal Processing, Pearson Education”, 4th edition.

References Books:

1. H. Monson Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley and Sons,Inc.2008.
2. G.JohnProakis, “Algorithms for Statistical Signal Processing”, Pearson Education, 2002.
3. G.Dimitris and G.Manolakis, “Statistical and Adaptive Signal Processing”, McGraw Hill, 2002.

EMBEDDED - C

I - Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To introduce the basic concepts of embedded system, processors, and programming languages.
- To make familiar with various issues interface, memory, and power consumption.

Learning Outcomes:

Students will be able to

- distinguish C and Embedded – C.
- select the processor, memory and operating system for an application.
- design and develop an application using Embedded–C.

UNIT - I: Programming embedded systems in C

Introduction to embedded system, selection: processor, programming language and operating system; steps in developing embedded software. Introducing the 8051 microcontroller family**:**external interface of the standard 8051, reset requirements, clock frequency and performance, memory issues, I/O pins, timers, interrupts, serial interface, power consumption

UNIT - II: Reading switches

Basic techniques for reading from port pins, reading and writing bytes, reading and writing bits (simple version), reading and writing bits (generic version), need for pull-up resistors, dealing with switch bounce, reading switch inputs (basic code), example: counting goats.

UNIT - III: Adding structure to the code

Object-oriented programming with C, the project header (MAIN.H), the port header (PORT.H), restructuring the goat-counting example.

UNIT - IV: Meeting real-time constraints

Introduction, creating 'hardware delays' using Timer 0 and Timer 1, generating a precise 50 ms delay, creating a portable hardware delay, use of Timer 2, need for 'timeout' mechanism, creating loop timeouts, testing loop timeouts, reliable switch interface, creating hardware timeouts, testing a hardware timeout

UNIT - V: Case study

Intruder alarm system:Introduction, key software components used, running the program, the software.

Text Books:

1. Michael J. Pont, "Embedded C", Pearson Education, 2nd Edition 2008.

Reference Books:

1. Michael Bass, "Programming Embedded Systems in C and C++", Oreilly, 2003.
2. Dreamtech Software Team, "Programming for Embedded Systems", Wiley-Dreamtech India Pvt. Ltd.

Elective - I

PRINCIPLES OF DIGITAL SYSTEM DESIGN

I – Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To introduce the principles of design of digital circuits using PLAs.
- To gain the knowledge of fault diagnosis in combinational and sequential circuits.
- To expose the students to finite state machines.

Learning Outcomes:

Students will be able to

- design a digital system.
- classify the PLDs and design digital circuits using PLAs.
- apply appropriate test generation techniques to find test vectors.
- conduct an experiment for fault detection.

UNIT - I: Minimization Procedures and CAMP Algorithm

Review on minimization of switching functions using tabular methods, K-map, QM algorithm, CAMP-I algorithm: phase I- determination of adjacencies, DA, CSC, SSMs and EPCs, phase II-passport checking, determination of SPC, CAMP-II algorithm: determination of solution cube, cube based operations, determination of selected cubes, introduction to cube based algorithms.

UNIT - II: Fault Diagnosis

Faults classes and models, fault diagnosis and testing, test generation, circuit under test methods- path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, D-algorithm, PODEM, random testing, transition count testing and signature analysis.

UNIT - III: State identification and Fault Detection Experiments

Experiments, homing experiments, synchronizing experiments, distinguishing experiments, adaptive distinguishing experiments, machine identification, fault detection experiments.

UNIT - IV: Programmable Logic Arrays and Design for Testability

Introduction to PLDs, PLA minimization, essential prime cube theorems, PLA folding, foldable compatibility matrix, the COMPACT algorithm, faults in PLAs, test generation, undetectable faults, design for testability, DFT schemes, built in self test.

UNIT - V: Synchronous and Asynchronous Sequential Circuits

Sequential circuits, the finite state model, memory elements and their excitation functions, synthesis of synchronous sequential circuits, capabilities and limitations of finite state machines, state equivalence and machine minimization, simplification of incompletely specified machines, fundamental mode circuits, synthesis, state assignment in asynchronous sequential circuits.

Text Books:

1. N. N. Biswas, “Logic Design Theory”, PHI, 2001. (Units: I, II, IV)
2. Z. Kohavi, “Switching and Finite Automata Theory”, TMH, 2nd Edition, 2001. (Units: III, V)

Reference Books:

1. Parag K.Lala, “Fault Tolerant and Fault Testable Hardware Design”, BS Publications, 2002.
2. Charles H. Roth, “Fundamentals of Logic Design”, Cengage Learning, 5th Edition, 2007.
3. Samuel C. Lee, “Digital Circuits and Logic Design”, PHI, 2001.

Elective - I

EMBEDDED REAL TIME OPERATING SYSTEMS

I - Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To impart the knowledge of embedded programming concepts.
- To familiarize with the real time operating system tools and their applications.

Learning Outcomes:

Students will be able to

- apply the concepts of embedded programming for real time applications.
- understand the techniques of testing and debugging of firmware.
- develop the networking applications using RTOS.

UNIT - I: Programming concepts and Embedded Programing in C & C^{++}

Software programming in assembly language(ALP) and high level language 'C', 'C' program elements, header, source files, processor directives, macros and functions, data types, data structures, modifiers, statements, loops, pointers, queues, stacks, lists and order lists and embedded programming in C^{++}.

UNIT - II: Software Engineering Practices in the Embedded Software Development Process

Software algorithm complexity, software development process life cycle and its models, software analysis, design, implementation, testing, validation and debugging, multiple processes in an application, problem of sharing data by multiple tasks and routines, inter process communication.

UNIT - III: Real Time Operating Systems

Operating system services, I/O subsystems, network operating systems, real time and embedded system operating systems, interrupt routines, handling of interrupt source, task scheduling models, interrupt latency and response times of the tasks as performance metrics, performance metric in scheduling models for periodic, sporadic and aperiodic tasks.

UNIT - IV: Real Time Operating System Programming Tools: µC/OS-II and Vx Works

Need of a well-tested and debugged real-time operating system (RTOS), use of µC/OS-II, Vxworks. Case study of coding for an automatic vending machine and automotive applications using µC/OS RTOS, Coding for sending application layer byte streams on a TCP/IP network using RTOS VxWorks.

UNIT - V: Middleware and application software

Middleware and its application, Networking Middleware driver, Application layer software, FTP Client Application, SMTP and E-mail, HTTP Client and Server and their examples.

Text Books:

1. Raj Kamal, "Embedded Systems-Architecture, Programming and Design", Tata McGraw HillPublications, 1st Edition, 2005. (Units: I to IV)
2. Tammy Noergaard "Embedded systems Architecture", Elsevier Publications 2ndEdition, 2005. (Unit: V)

Reference Books:

1. Jean J.Labrosse, "Embedding system building blocks ", CMP publishers. 2nd Edition
2. Rob Williams," Real time Systems Development", Butterworth Heinemann Publications.
3. Dr. K.V.K.K. Prasad, "Embedded/Real-Time Systems" Dream Tech Publications.

Elective - I

ARM ARCHITECTURE AND PROGRAMMING

I - Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Pre-requisite:

- Basic knowledge on microcontroller 8051, programming (preferably C), computer architecture and computer logic design.

Course Objectives:

- To introduce the basic concepts of ARM architecture and processor families.
- To familiarize the various concepts of registers, instruction sets, interrupts and vector tables.
- To impart the ARM programming skills.

Learning Outcomes:

Students will be able to

- understand the architecture of the ARM microcontrollers and ARM processor families.
- apply the concepts of registers, thumb instruction sets, memory organization and Interrupts.
- develop a real time application using ARM.

UNIT - I: ARM Architecture

ARM design philosophy, registers, program status register, instruction pipelines, interrupts and vector table, cache architecture, polices, flushing and caches, MMU, page tables, translation, access permissions, context switch.

UNIT - II: ARM Programming Model – I

Instruction set: data processing instructions, addressing modes, branch, load, store instructions, program status register instructions, conditional instructions.

UNIT - III: ARM Programming Model – II

Thumb instruction set: register usage, other branch instructions, data processing instructions, single and multi-register load-store instructions, stack, software interrupt instructions. .

UNIT - IV: **ARM Programming**

C programs using function calls, pointers, structures, integer and floating point arithmetic, assembly code using instruction scheduling, register allocation, conditional execution and loops.

UNIT - V: **Embedded ARM Applications**

ARM processor families,VLSI ruby II advanced communication processor, ISDN subscriber processor, one C™ VWS22100 GSM chip, Ericson-VLSI Bluetooth baseband controller, ARM7500 and ARM7500FE.

Text Books:

1. Andrew N. Sloss, Dominic Symes, Chris Wright, “ARM Systems Developers Guide - Design & Optimizing System Software”, Elsevier,2004. (Units: I to IV)
2. Steve furber, “ARM System-on-Chip Architecture”, Addison Wesley, 2nd Edition. (Unit: V)

References Books:

1. Jonathan W. Valvano – Brookes / Cole , “Embedded Microcomputer Systems, Real Time Interfacing”, Thomas Learning, 1999.
2. John B. Peatman, “Designing with PIC Microcontrollers”, PH Inc, 1998.

Elective - II

EMBEDDED SOFTWARE CONCEPTS

I – Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To introduce advanced–C and Embedded –C concepts.
- To familiarize with Linux OS and embedded protocols.

Learning Outcomes:

Students will be able to

- write programs to implement system calls, scheduling and threading.
- develop applications using Linux software development tools.
- develop a client server model with concurrent and iterative approaches.

UNIT – I: Linux and Advanced – C/Embedded-C concepts

Introduction to Linux, basic Linux commands, gcc compiler, storage classes, arrays, functions, structures, unions, pointers, function pointers, program with multiple C files, bit wise operations, files (standard I/O library functions), Linux executable image contents, text/code, read only data, data, BSS, development tools in Linux, make file, GNU debugger.

UNIT – II: Linux System Programming - I

Linux operating systems concepts, file descriptor, system calls, file I/O system calls, multi-threading, synchronization and mutual exclusion for threads, multi-processing process related system calls.

UNIT – III: Linux System Programming – II

Signals, inter process communication: pipes, FIFO (named pipes), message queues, semaphores, shared memory.

UNIT – IV: Network Programming

Concepts of socket / socket pair, client and server, connectionless and connection oriented protocols (UDP/TCP); socket calls for UDP server and client, TCP server and client; concurrent/iterative server and TCP/IP socket programming.

UNIT - V: Embedded Protocols

Embedded protocols, I^2C/SPI, Linux I^2C tools, I^2C detect, I^2C set.

Text Books:

1. John.W.Perry, “Advanced C Programming by Example”. (Unit: I)
2. Michael Kerrisk, “The Linux Programming Interface”. (Units: II, III)
3. Kurtwall "Linux Programming by Example". (Unit: IV)
4. Vahid Frank " Embedded System Design". (Unit: V)

References Books:

1. Robert Love, “Linux System Programming”.

Elective - II

ADVANCED COMPUTER ARCHITECTURE

II – Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To impart knowledge on basic quantitative principles of computer design and performance measurements.
- To familiarize with the structure of modern compilers and Networks.

Learning Outcomes:

Students will be able to

- understand instruction parallelism in high performance processors.
- apply synchronization and memory consistency models for multi-threading operations
- understand principles for the design of local area, storage area and wide area networks.
- design a cluster.

UNIT - I: Instruction Set Principles

Classifying instruction set architectures, memory addressing, addressing modes for signal processing, types and size of operands, operands for media and signal processing, operation in the instruction set, instructions for control flow, encoding an instruction set.

UNIT - II: Instruction Level Parallelism and its Dynamic Exploitation

Instruction level parallelism concepts and challenges, overcoming data hazards with dynamic scheduling, reducing branch costs with dynamic hardware prediction, high performance instruction delivery, taking advantage of more ILP with multiple issues, hardware based speculation.

UNIT - III: Memory Hierarchy Design

Cache performance, reducing-cache miss penalty, miss rate, miss penalty or miss rate via parallelism; main memory and organization for improving performance, memory technology, virtual memory, protection and examples of virtual memory.

UNIT - IV: Multi processors and Thread level parallelism

Characteristics of application domains, symmetric shared memory architectures, performance of symmetric shared memory multiprocessors, distributed shared memory architectures, performance of distributed shared memory multiprocessors, synchronization.

UNIT - V: Interconnection networks and clusters

A simple network, interconnection network media, connecting more than two computers, network topology, practical issues for commercial interconnection networks, examples of interconnection networks, internetworking, crosscutting issues for interconnection networks, clusters, designing a cluster.

Text Books:

1. John L. Hennessy, David A.Patterson, "Computer Architecture- A Quantitative Approach", Elsevier Publications, 3rd Edition. (Units: I, II,III,IV)
2. Richard Y. Kain, "Advanced Computer Architecture- A System Design Approach", PHI, 1st Edition. (Unit: V)

Reference Books:

1. Michael J. Flynn, "Computer Architecture Pipelined & Parallel processing Design" Narosapublication, 1st Edition.
2. Kai Hwang &Naresh Jot Wani, "Advanced Computer Architecture Parallelism, Scalability, Programmability" TMH, 2nd Edition.

Elective - II

HARDWARE SOFTWARE CO-DESIGN

I - Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To introduce the concepts of hardware/software co-design
- To familiarize with various target architectures and methods of prototyping, emulation and verification tools.

Learning Outcomes:

Students will be able to

- demonstrate the knowledge of the fundamental principles of hardware/ software co-design techniques.
- apply methods of prototyping and emulation on target devices.
- perform hardware and software co-design using verification tools.

UNIT - I: Co- design issues

Hardware/Software co-design, motivation for co-design, co-design models, architectures, languages, generic co-design methodology.

UNIT - II: Prototyping and Emulation

Prototyping and emulation-techniques, environments, future developments; architecture specialization techniques, system communication infrastructure.

UNIT - III: Target architectures

Target architectures and application system classes, architecture for control dominated systems (8051 and Motorola processors), data dominated systems (ADSP21060, TMS320C60), mixed systems.

UNIT - IV: Compilation techniques and embedded processor architectures

Modern embedded architectures, embedded software development needs, compilation technologies, practical considerations in a compiler development environment.

UNIT - V: Languages for system level specification and design

System-level specification, design representation for system level synthesis, system level specification languages, heterogeneous specification and multi-language co-simulation.

Text Books:

1. Jorgen Staunstrup, Wayne Wolf, “Hardware / software co- design Principles and Practice”, Springer, 2009.

Reference Books:

1. Patrick Schaumont, “A Practical Introduction to Hardware/Software Co-design”, 2nd Edition,2012.
2. R. Gupta,”Co-synthesis of Hardware and Software for Embedded Systems”, Kluwer Academic Publishers, 1995.

HARDWARE DESCRIPTION LANGUAGE LAB

I - Semester

Practical	: 6	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To familiarize with the design of various combinational and sequential circuits using Verilog /VHDL.

Learning Outcomes:

Students will be able to

- make use of CAD tools to simulate and synthesize various combinational and sequential circuits.
- analyze various parameters like delay, power, and area.

List of Experiments:

A minimum of TWELVE experiments required to be perfomred.
Open ended experiment is mandatory.

1. Address decoder
2. Carry skip /Carry select adders
3. Multipliers
4. Latches
5. Barrel shifters
6. Random counter
7. Synchronous RAM/ROM
8. Moore/Mealy FSM
9. ACS unit
10. MAC unit
11. DCT
12. FIR/IIR filter
13. I^2C bus protocol
14. ALU
15. UART
16. Design and implement a simple processor/controller on FPGA-Open ended experiment.

CMOS ANALOG AND DIGITAL DESIGN

II – Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Pre-requisite: Basic knowledge on analog and digital electronics.

Course Objectives:

- To introduce to CMOS models.
- To familiarize with various CMOS analog and digital circuits.

Learning Outcomes:

Students will be able to

- understand the MOS device models.
- design various combinational and sequential circuits using CMOS.
- realize different memory circuits.
- analyze and design various CMOS analog circuits.

UNIT - I: MOS Devices and Modeling

MOS transistor structure, MOS transistor V-I characteristics, interconnect parameters, secondary effects, static and dynamic behavior of CMOS inverter, power, energy and energy delay, CMOS device modeling–small and large signal models.

UNIT - II: Combinational MOS Logic Circuits

Complementary CMOS, ratioed logic-pseudo-NMOS logic, Differential Cascade Voltage Switch Logic (DCVSL), pass transistor logic, inverse pass transistor logic, transmission gates, domino CMOS logic.

UNIT - III: Sequential MOS Logic Circuits

Behavior of bi-stable elements, latches and flip-flops using CMOS and transmission gates, semiconductor memories:types, RAM array organization, DRAM – types, operation, leakage currents in DRAM cell and refresh operation, SRAM operation, leakage currents in SRAM cells, flash Memory- NOR flash and NAND flash.

UNIT - IV: Analog CMOS Sub-Circuits and Amplifiers

MOS switch, MOS diode, MOS active resistor, current sinks and sources, current mirrors-current mirror with beta helper, CMOS amplifiers: common source, common drain, common gate, cascode amplifiers, and differential amplifiers.

UNIT - V: CMOS Operational Amplifiers

Performance parameters, one-stage and two-stage op-amps, gain boosting, power supply rejection ratio of two-stage op amps, cascode op amps, measurement techniques of op- Amp.

Text Books:

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits – A Design Perspective", 2nd Ed., PHI.(Units: I, II, III)
2. Behzad Razavi," Design of Analog CMOS Integrated Circuits", TMH Edition, 2001. (Units: I, IV, V)

Reference Books:

1. David A. Johns, Ken Martin, "Analog Integrated Circuit Design", Wiley Student Edition, 2013.
2. Ashok K Sharma, "Semiconductor Memories, Technology, Testing and Reliability".
3. Keeth and Baker, "DRAM Circuit Design", Wiley 2007.

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

II – Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To familiarize with the architecture and interfacing of TMS320C54XX and ADSP 2100 processors.

Learning Outcomes:

Students will be able to

- apply the concepts of sampling, DFT and filters.
- calculate DSP computational errors.
- understand the architectural features of DSP processors.
- interface I/O and memory devices with DSP processors.

UNIT - I: Introduction to DSP

Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT) Radix-2, Digitalfilters (FIR and IIR), Decimation and interpolation.

Computational Accuracy in DSP Implementations

Number formats for signals and coefficients in DSP systems, dynamic range and precision, sources of error in DSP implementations, A/D conversion errors, DSP computational errors, D/A conversion errors, compensating filter.

UNIT - II: Architecture for Programmable DSP Devices

Basic architectural features, DSP computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

UNIT - III: Digital Signal Processor - TMS320C54XX

Data addressing modes, memory space, program control, instructions and programming, on-chip peripherals, interrupts and pipeline operations.

UNIT - IV: Peripheral Interfacing with TMS320C54XX

Interfacing memory and I/O peripherals to programmable DSP devices, memory space organization, external bus interfacing signals, memory interface, parallel I/O interface, programmed I/O, interrupts, direct memory access (DMA).

UNIT - V: Digital Signal Processor - ADSP 2100

ALU and MAC block diagram, shifter instruction, base architecture,block diagrams and function of program sequencer, barrel shifter and data address generator.

Text Books:

1. Avtar Singh and S.Srinivasan,"Digital Signal Processing", Thomson Publications, 2004. (Units: I to IV)
2. ADSP-2100 Family User's Manual by the Applications Engineering Staff of Analog Devices, DSP Division, Third Edition (9/95), September 1995. (Unit: V)

Reference Books:

1. Jonatham Stein, "Digital Signal Processing", John Wiley, 2005.
2. B. Venkataramani and M. Bhaskar, "Digital Signal Processors, Architecture, Programming and Applications", 2002, TMH.

EMBEDDED COMPUTING

II - Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To familiarize with embedded platform, processor architectures and power optimization techniques.
- To impart the knowledge of parallel processing and networking basics.

Learning Outcomes:

Students will be able to

- make intelligent choices between hardware/software tradeoffs.
- understand embedded platform and processor architectures.
- apply power optimization and parallel processing techniques to embedded system design.
- develop an application using an Intel Atom processor.

UNIT - I: Embedded Platform Architecture

Embedded platform overview and characteristics, volatile memory technologies, non- volatile storage, device interface-high performance, universal serial bus, device interconnect – low performance; general purpose input/output, power delivery.

UNIT - II: Embedded Processor Architecture

Basic execution environment, application binary interface, processor instruction classes, exceptions/interrupts model, vector table structure, exception frame, masking and acknowledging interrupts, interrupt latency, memory mapping and protection, MMU and processes, memory hierarchy, Intel atom micro architecture

UNIT - III: Power Optimization and Parallel Processing

Power optimization: Basics, power profile of an embedded computing system, constant versus dynamic power, simple model of power efficiency, advanced configuration and power interface, optimizing software for power performance

Parallel processing: Types and levels of parallelism, classification of parallel architectures, basic parallel techniques.

UNIT IV: Networking Connectivity

Networking Basics:

Sockets, TCP/IP Networking, Ethernet, Wi-Fi and IEEE 802.11, Bluetooth.

Platform and Content Security:

Principles, concepts and building blocks, platform support for security.

UNIT V: Intel Architecture

Intel Atom E6XX series platforms, multi-radio communications design, multimedia design, modular references.

Text Books:

1. Peter Barry and Patrick Crowley , "Modern Embedded Computing", 1st Edition, Elsevier/Morgan Kaufmann, 2012. (Units I to V)
2. DezsoSima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architectures", Pearson Education Ltd. (Unit III)

Reference Books:

1. Joseph A. Fisher, Paolo Faraboschi and Cliff Young , "Embedded Computing – A VLIW Approach to Architecture, Compilers and Tools",Elsevier/Morgan Kaufmann, 2005
2. Kai Hwang, "Advanced computer architecture –Parallelism, Scalability Programmability", McGraw Hill,1993

WIRELESS SENSOR NETWORKS

II – Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To familiarize the students with wireless sensor networks and their architectures.
- To expose students to MAC, link layer and routing protocols.

Learning Outcomes:

Students will be able to

- understand the design considerations of wireless sensor networks for various applications.
- distinguish the functions of different layers.
- apply appropriate routing protocols.
- use various data centric and aggregation techniques for reliable data transfer.

UNIT - I: Overview of Wireless Sensor Networks and Architectures

Introduction to sensor networks, comparison of sensor network with adhoc network, challenges for sensor networks, advantages, applications and enabling technologies for wireless sensor networks. Single-node architecture - hardware components, energy consumption of sensor nodes, operating systems and execution environments, network architecture - sensor network scenarios, design principles for WSNs, gateway concepts.

UNIT - II: Physical Layer

Introduction, wireless channel and communication fundamentals – frequency allocation, modulation and demodulation, wave propagation effects and noise, channels models, spread spectrum communication, packet transmission and synchronization, quality of wireless channels and measures for improvement, physical layer and transceiver design considerations in wireless sensor networks- energy usage profile, choice of modulation scheme, dynamic modulation scaling, antenna considerations.

UNIT - III: MAC Protocols and Link Layer Protocols

Fundamentals of wireless MAC protocols, low duty cycle protocols and wakeup concepts, contention based protocols, schedule based protocols, link layer protocols- fundamental task and requirements, error control, framing, link management.

UNIT - IV: Routing Protocols for Wireless Sensor Networks

Introduction, background, data dissemination and gathering, routing challenges and design issues in wireless sensor networks, routing strategies in wireless sensor networks.

UNIT - V:

Data Centric and Content Based Networking and Transport layer

Introduction, data centric routing, data aggregation, data centric storage, the transport layer and qos in wireless sensor networks, coverage and deployment, reliable data transport single packet delivery, block delivery, congestion control and rate control.

Text Books:

1. Holger Karl and Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks", John Wiley, 2005. (Units: I, II, III, V)
2. Kazem Sohraby, Daniel Minoli and Taieb Znati, " Wireless Sensor Networks Technology, Protocols and Applications", John Wiley & Sons, 2007. (Unit: IV)

Reference Books:

1. Feng Zhao and Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
2. Anna Hac, "Wireless Sensor Network Designs", John Wiley, 2003.
3. C.S.Raghavendra, Krishna M.Sivalingam and TaiebZnati, "Wireless Sensor Networks", Springer publication, 2004.

Elective - III

SENSORS AND ACTUATORS

II - Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To familiarize with various types of sensors and actuators.
- To expose the design aspects of a smart sensor system.

Learning Outcomes:

Students will be able to

- understand the principles of different sensors and actuators.
- use the sensors and actuators in practical applications.

UNIT - I: Introduction

Measurement systems, control systems,microprocessor based controllers,single and multichannel data acquisition systems.

UNIT - II: Mechanical and Electromechanical Sensors

Selection of a sensor, sensors for displacement- resistance, capacitance and LVDT; strain gauges; resistance thermometers,thermocouples and thermistors, ultrasonic sensors.

UNIT - III: Magnetic Sensors

Introduction, principles, Hall Effect sensors, eddy current sensors, electromagnetic flow meter, switching magnetic sensors, SQUIDs.

UNIT - IV: Smart Sensors

Introduction, primary sensors, excitation, amplification, filters, converters, compensation, information coding processing, data communication, the automation.

Sensors Applications: Introduction, on-board automobile (automotive) sensors, home appliance sensors, aerospace sensors.

UNIT - V: Actuators

Actuation systems, pneumatic and hydraulic systems, directional control valves, pressure control valves, cylinders, process control valves, rotary actuators.

Mechanical Actuation Systems:Types of motion, kinematic chains, cams, gears, ratchet and pawl, belt and chain drives, bearings.

Electrical Actuation Systems: D.C. motors, A.C. motors, stepper motors.

Text Books:

1. D. Patranabis, “Sensors and Transducers”,PHI Learning PrivateLimited, 2nd Edition, 2006. (Units: II, III, IV)
2. W. Bolton,”Mechatronics”,Pearson Education Limited,3rd Edition,2003. (Unit: I, V)

Reference Books:

1. D. Patranabis,”Sensors and Actuators”, PHI, 2nd Edition,2013.
2. C.S.Rangan,”Instrumentation devices and systems”, TMH, 2nd Edition, 2002.

Elective - III

SYSTEM ON CHIP DESIGN

I – Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Pre-requisite:

Basic knowledge on analog and digital electronics, communications, micro processor and microcontroller, embedded and real time systems.

Course Objectives:

- To provide an overview on System-On-Chip design technology.
- To introduce components in a typical SoC system.
- To familiarize with the concept of different processor cores.

Learning Outcomes:

Students will be able to

- understand various memories and interconnects used in SoCs.
- design SoCs for various applications.
- perform SoC customization, prototyping and verification.

UNIT - I: Introduction to Architecture Designs

Architecture and design issues of SoC,hardware software co-design,co-design flow, core libraries, EDA tools and web pointers.

UNIT - II: Design Methodology for Logic Cores

SoC design flow, guidelines for design reuse, synchronous design, memory and mixed-signal design, on-chip buses, clock distribution,design process for soft,firm and hard cores,system integration.

UNIT - III: Design Methodology for Memory and Analog Cores

Embedded memories and design methodology,specifications of analog circuits, circuit techniques, memory compiler, simulation models, analog-to-digital converter, digital-to-analog converter , phase-locked loops, high speed circuits.

UNIT - IV: Design Validation

Core-Level validation, core validation plan, test benches, core-level timing verification, core inter face verification, protocol verification, gate-level simulation, SoC design validation, co-simulation, emulation, hardware prototypes.

UNIT - V: Core and SoC Design Examples

Micro processor cores, V830 R/AV super scalar RISC core, design of power PC 603e G2 core, memory core generators, Core Integration and on-chip bus, examples of SoC, media processors, and testability of set-top box SoC.

Text Books:

1. Rochit Raj Suman,"System-on-a-chip: Design and Test", Artech House, 2000.

Reference Books:

1. Jason Andrews – Newnes "Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) ", BK and CDROM.
2. Prakash Rashinkar, Peter Paterson and Leena Singh L "System on Chip Verification – Methodologies and Techniques", Kluwer Academic Publishers, 2001.
3. Ricardo Reis,"Design of System on a Chip: Devices and Components", 1st Ed., Springer 2004.

Elective - III

DESIGN OF FAULT TOLERANT SYSTEMS

II – Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To familiarize with basic concepts of fault tolerant systems.
- To impart knowledge on testing of combinational and sequential circuits.

Learning Outcomes

Students will be able to

- design different redundant systems and self - checking circuits.
- compare different design techniques of testability.
- generate test pattern for BIST.

UNIT - I: Basic Concepts

Reliability concepts, failureand faults, reliability and failure rate, relation between reliability and meantime between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.

UNIT - II: Fault Tolerant Design

Basic concepts – static, dynamic, hybrid, triple modular redundant system, self-purging redundancy, Sift-out Modular Redundancy (SMR), SMR configuration, use of error correcting code, time and software redundancies, self-checking circuits, design of totally self-checking checkers-checkers using m out of n, Berger, and low cost residue codes.

UNIT - III: Fail - Safe Design

Strongly fault secure circuits, fail-safe design of sequential circuits using Berger code, totally self-checking PLA design, LFSR as signature analyzer, multiple-input signature register.

UNIT - IV: Design for Testability

Basic concepts of testability, controllability and observability, the Reed-Muller's expansion technique, OR-AND-OR design, use of control and syndrome testable design, scan register, classic scan design, Level Sensitive Scan Design (LSSD).

UNIT - V: Built-In Self-Test (BIST)

Test pattern generation for BIST exhaustive testing, pseudorandom testing, pseudo exhaustive testing, constant weight patterns, generic offline BIST architecture.

Text Books:

1. Parag K. Lala , "Fault Tolerant & Fault Testable Hardware Design", BS Publications, 2002.

Reference Books:

1. M. Abramovici, M.A. Breues, A. D. Friedman, "Digital Systems Testing and Testable Design", Jaico publications, 2008.

Elective - IV

MICRO ELECTRO MECHANICAL SYSTEMS

II - Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Pre-requisite :

Basic knowledge in dynamics, mechanics of materials, electro magnetism and IC fabrication processes.

Course Objectives :

- To familiarize with fabrication of MEMS.
- To emphasize the various applications of MEMS.

Learning Outcomes :

Students will be able to

- understand the fundamental fabrication processes used in MEMS.
- use MEMS for various applications.

UNIT - I: Introduction to MEMS and Micro electronic Technologies

Historical background and evolution of MEMS, emergence of micro machines, material properties, wafer preparation, monolithic processing and mounting, PCB technologies, hybrid and MCM technologies.

UNIT - II: Silicon Bulk Micromachining

Isotropic and orientation-dependent wet etching, etch-Stop techniques, dry etching, buried oxide process, silicon fusion bonding, and anodic bonding.

UNIT - III: Silicon Surface Micromachining

Sacrificial layer technology, material systems in sacrificial layer technology, surface micromachining using plasma etching, combined IC technology and anisotropic wet etching, processes using both bulk and surface micromachining, adhesion problems in surface micromachining, surface versus bulk micromachining.

UNIT - IV: Micro stereo Lithography (MSL)

Micro stereo lithography, scanning method, two-photon MSL, other MSL approaches, projection method, polymeric MEMS architecture with silicon, metal and ceramics, combined silicon and polymeric structures.

UNIT - V: MEMS Applications

Thermal sensors (resistive temperature, micro thermo couples), radiation sensors (photoconductive, photovoltaic), mechanical sensors(pressure, flow, gyro meters, accelerometers).

Micro actuators: transducers with mechanical output, electrostatic forces, electrostatic micro actuator on figurations, piezoelectric micro actuators.

Text Books:

1. Julian W.Gardner, Vijay. K.Varadhan, Osama O.Awadelkahn,"Micro sensors, MEMS, and Smart Devices", Wiley Publishers, 2001.

Reference Books:

1. G. Korvink, Oliver Paul, "MEMS: A Practical Guide to Design, Analysis, and Applications", Spinger, 2006. (Micro Actuators)
2. Nitaigour Mahalik,"MEMS" , Tata McGraw Hill,2007 .
3. Rai Chaoudhary, "MEMS and MOEMS Technology and Applications", PHI Learning, 2000.

Elective - IV

EMBEDDED NETWORKING

II - Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To impart knowledge about CAN protocol.
- To impart knowledge about USB protocol.

Learning Outcomes:

Students will be able to

- implement CAN protocol in embedded system design.
- implement USB protocol in embedded system design.

UNIT - I: Embedded Networking and CANopen standard

Embedded networking, code requirements, communication requirements, introduction to CANopen from the application level, CANopen standard, object dictionary, electronic data sheets and device configuration files, service data objectives, network management, CANopen example configurations, CANopen messages.

UNIT - II: CANopen Configuration

Evaluating system requirements, choosing devices and tools, configuring single devices, overall network configuration, network simulation, network commissioning, advanced features and testing.

UNIT - III: Underlying Technology: CAN

CAN overview and introduction, selecting a CAN controller, CAN development tools.

UNIT - IV: Implementing CANopen

Communication layout and requirements, comparison of implementation methods, micro CANopen, CANopen source code, conformance test, design cycle.

UNIT - V: USB Bus Protocol

Introduction, speed identification on the bus, states, bus communication: packets, data flow types, enumeration; PIC 18 microcontroller USB interface.

Text Books :

1. GlafP.Feiffer, AndrewAyre and Christian Key old, “Embedded networking with CAN and CANopen” Embedded System Academy 2005. (Units: I to IV)
2. DoganIbrahim “Advanced PIC microcontroller projects in C from USB to RTOS with the PIC18F series”, Elsevier 2008. (Unit: V)

Reference Books :

1. Marco Di Natale, HaiboZeng, Paolo Giusto, ArkadebGhosal “Understanding and Using the Controller Area Network Communication Protocol: theory and practice” ,Springer 2012.
2. Jan Axelson”USB complete, The developer’s guide” Lakeview research LLC,4th edition.

Elective - IV

CPLD AND FPGA ARCHITECTURES

I – Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To introduce the students the architectures of CPLD and FPGA devices.
- To expose the students to design tools.

Learning Outcomes:

Students will be able to

- comprehend FPGA and CPLD technologies
- optimize the chip area, interconnect wire length and delays
- design systems using One- Hot design method.

UNIT - I: Programmable Logic Devices

ROM, PAL, PLA, Xilinx cool runner XCR3064XL CPLD and FPGA – features, architectures, programming, applications and implementation of MSI circuits using programmable logic devices.

UNIT - II: SRAM Programmable FPGAs

Programming technology, device architectures of Xilinx XC2000, XC3000, XC4000 FPGAs.

UNIT - III: Antifuse Programmable FPGAs

Programming technology, device architectures of Actel ACT1, ACT2, ACT3 FPGAs and their speed performance.

UNIT - IV: Finite State Machines - Architectures

Top down design, state transition table, state assignments for FPGAs, realization of state machine charts using PALs, alternative realization of state machines using microprogramming, linked state machine, FSM architectures centered around non-registered PLDs and shift registers, petrinets for state machines – basic concepts and properties, extended petrinets for parallel controllers.

UNIT - V: Design Methods

One – hot design method-use of ASMs, applications, metastability and synchronization.

System - Level Design: Controller, data path, and functional partition, design of a parallel to serial adder/subtractor control system.

Text Books:

1. Stephen M. Trimberger, "Field Programmable Gate Array Technology", Springer Publications, 2007. (Units: II, III)
2. Richard F.Tinder, "Engineering Digital Design", Academic Press, 2nd Edition, 2001. (Units: I, IV, V)

Reference Books:

1. Charles H.Roth, "Fundamentals of Logic Design", Jaico Publishing House, 5th Edition. (Device architecture of XCR 3064XL CPLD)
2. Stephen D.Brown, R.J.Francis, J.Rose, Z.G.Vranesic, "Field Programmable Gate Arrays", BS Publications, 2007.

EMBEDDED SYSTEMS LAB

II - Semester

Practical	: 6	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

- To familiarize with the high level language programming and I/O interfacing.
- To expose to wireless communication protocols and Linux operating system.

Learning Outcomes:

Students will be able to

- interface I/O devices to various processors.
- develop the source code in Linux environment.

List of Experiments:

A minimum of **EIGHT** experiments from part-A and **TWO** from part-B are to be performed. Open ended experiments are mandatory.

PART - A :

High level language programming and porting it on a processor

1. Basic arithmetic operations
2. ASCII to decimal vice versa conversion
3. Read switch status and display on LEDs
4. Stepper motor control
5. Serial communication using UART
6. Keyboard interfacing with LCD display
7. Seven-segment display control
8. FSM concept of traffic light controller interface with ARM processor.
9. Develop and implement an application using ARM processor.
10. Implement the developer board as a modem for data communication between two PCs.–Open ended experiment

PART - B :

Experiments on wireless communication protocols and open source software

1. File transfer application using GSM/GPS interface
2. Develop source code for inter process communication (mutex, semaphore etc.) using Linux operating system.
3. Develop source code for task scheduling (FIFO/LIFO/SJF) using Linux operating system.
4. Implementation of a wireless communication protocol on an embedded system - Open ended experiment.