ACADEMIC REGULATIONS
COURSE STRUCTURE
AND
DETAILED SYLLABUS

EMBEDDED SYSTEMS

Department of
Electronics and Communication Engineering

M.Tech Two Year Degree Course

(Applicable for the batch admitted from 2017-18)

GUDLAVALLERU ENGINEERING COLLEGE

(An Autonomous Institute with Permanent Affiliation to JNTUK, Kakinada)

Seshadri Rao Knowledge Village

GUDLAVALLERU - 521 356, Krishna District, Andhra Pradesh

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VISION & MISSION OF THE COLLEGE

Vision

To be a leading institution of engineering education and research, preparing students for leadership in their fields in a caring and challenging learning environment.

Mission

- To produce quality engineers by providing state-of-the-art engineering education.
- To attract and retain knowledgeable, creative, motivated and highly skilled individuals whose leadership and contributions uphold the college tenets of education, creativity, research and responsible public service.
- To develop faculty and resources to impart and disseminate knowledge and information to students and also to society that will enhance educational level, which in turn, will contribute to social and economic betterment of society.
- To provide an environment that values and encourages knowledge acquisition and academic freedom, making this a preferred institution for knowledge seekers.
- To provide quality assurance.
- To partner and collaborate with industry, government, and R and D institutes to develop new knowledge and sustainable technologies and serve as an engine for facilitating the nation's economic development.
- To impart personality development skills to students that will help them to succeed and lead.
- To instil in students the attitude, values and vision that will prepare them to lead lives of personal integrity and civic responsibility.
- To promote a campus environment that welcomes and makes students of all races, cultures and civilizations feel at home.
- Putting students face to face with industrial, governmental and societal challenges.

VISION & MISSION OF THE DEPARTMENT

Vision

To be a leading centre of education and research in Electronics and Communication Engineering, making the students adaptable to changing technological and societal needs in a holistic learning environment.

Articulations

- To be a leading centre of education and research hub in Electronics and Communication Engineering with holistic learning environment.

- Students to be adaptable for the changes in technology and societal needs.
- Students to be recognized and valued for their commitment to excellence and enthusiasm for learning..

Mission:

- To produce knowledgeable and technologically competent engineers for providing services to the society.
- To have a collaboration with leading academic, industrial and research organizations for promoting research activities among faculty and students.
- To create an integrated learning environment for sustained growth in electronics and communication engineering and related areas.

Articulations

- To craft the graduates knowledge and technologically competent engineers for providing services to the society.
- To have alliance with leading academicians, industries and research organizations and encourage the faculty and students for performing research activities.
- To develop a multidiscipline learning environment for continuous growth in electronics and communication engineering and its associated fields.

III. PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

To make the graduates of M. Tech Programme in Embedded Systems

PEO-I : Identify and use appropriate modern tools to solve real world problems in Embedded Systems domain.

PEO-II : Develop an ability of writing and presenting a substantial technical report/ document and demonstrate degree of mastery over the area of specialization.

PEO-III: Inculcate self learning to pursue research career in relevant areas.

IV. PROGRAM OUTCOMES (POs)

PO-1 : An ability to independently carry out research /investigation and development work to solve practical problems.

PO-2 : An ability to write and present a substantial technical report/document.

PO-3 : Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program.

V. ACADEMIC REGULATIONS

Applicable for the students of M.Tech from the Academic Year 2017-18.

1. Duration of the Program

The duration of the program is two academic years consisting of four semesters. However, a student is permitted to complete the course work of M.Tech program in the stipulated time frame of four academic years from the date of joining.

2. Minimum Instruction Days

Each semester consists of a minimum of ninety instruction days.

3. Program Credits

Each specialization of the M.Tech programs is designed to have a total of 70 credits and the student shall have to complete the two year course work and earn all the 70 credits for the award of M.Tech Degree.

4. Attendance Regulations

4.1 A student shall be eligible to appear for Semester End Examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.

4.2 Condoning of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester will be considered for genuine reasons such as medical grounds and participation in co-curricular and extra-curricular activities and shall be granted only after approval by the College Academic Committee. Student should submit application for medical leave along with medical certificate from a registered medical practitioner within three days from reporting to the class work after the expiry of the medical leave. In case of participation in co-curricular and extra-curricular activities, either in the college or other colleges, students must take prior written permission from HoD concerned and should also submit the certificate of participation from the organizer of the event within three days after the completion of the event. Only such cases will be considered for condoning attendance shortage.

4.3 A student shall be eligible to claim for condonation of attendance shortage only once during the two years (four semesters) course work.

4.4 A student will not be promoted to the next semester unless he satisfies the attendance requirement of the current semester. He may seek re-admission for that semester when offered next.

4.5 Shortage of Attendance below 65% in aggregate shall in *NO* case be condoned.

4.6 Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examination of that semester and their registration shall stand cancelled.

4.7 A fee stipulated by the college shall be payable towards condoning attendance shortage.

5. Examinations and Scheme of Evaluation

5.1 Theory Courses :

Each theory course shall be evaluated for a total of 100 marks, consisting of 40 marks for internal assessment and 60 marks for semester end examination.

Internal Assessment:

i) Of 40 marks for internal assessment, 10 marks are for continuous assessment in the form of two assignments and 30 marks are based on two mid-term examinations.

ii) Each assignment carries 10 marks and the average of two assignments shall be taken as the marks for continuous assessment.

iii) Each mid-term examination is conducted for 40 marks with two hours duration. Each mid-term examination consists of four questions, each for 10 marks. All the questions need to be answered.

iv) Sum of the75% marks of better scored mid-term examination and 25% marks of less scored mid-term examination are scaled down for 30 marks.

v) For the project based theory course, the distribution of 40 marks for internal evaluation shall be 20 marks for theory, based on two mid- term examinations and 20 marks for project. Each mid-term examination is conducted for 40 marks with two hours duration. Each mid-term examination consists of two questions, each for 20 marks, with internal choice. All the questions need to be answered. Sum of the 75% marks of better scored mid-term examination and 25% marks of less scored mid-term examination are scaled down for 20 marks.

External Assessment:

i) Semester End Examination will have 8 questions, each for 12 marks, out of which 5 questions are to be answered.

ii) For the project based theory course, semester end examination will have three questions, each for 20 marks, with internal choice. All the questions need to be answered. There will be no external assessment for project component.

5.2 Laboratory Courses :

i) For practical subjects the distribution shall be 40 marks for Internal Evaluation and 60 marks for the End-Examinations. There shall be continuous evaluation by the internal subject teacher during the semester for 40 internal marks. Of the 40 marks for internal, 25 marks shall be for day-to-day performance (15 marks for day-to-day evaluation and 10 marks for Record) and 15 marks shall be evaluated by conducting an internal laboratory test towards the end of semester.

ii) Semester end examination shall be conducted by an internal examiner and an external examiner for 60 marks.

5.3 (a) Seminar:

i) For seminar, a student under the supervision of a faculty member, shall collect the literature on an advanced topic related to his specialization and critically review the literature and submit it to the department in a report form towards the end of semester and shall make an oral presentation before the Departmental Review Committee consisting of the supervisor and a senior faculty member / Head of the Department. There shall be an internal evaluation for 100 marks in the form of viva-voce examination and assessment of report and its presentation. There will be NO external evaluation.

ii) If a candidate fails to secure the minimum marks prescribed for successful completion, he has to re-register by paying the prescribed fee at the beginning of subsequent semester(s). He has to submit a fresh report towards the end of that semester and appear for evaluation by the committee.

(b) Term Paper:

i) For term paper, a student under the supervision of a faculty member, shall collect the literature on an advanced topic related to his specialization and critically review the research papers and submit it to the department in publication form towards the end of semester and shall make an oral presentation before the Departmental Review Committee consisting of the supervisor and a senior faculty member / Head of the Department. There shall be an internal evaluation for 100 marks in the form of viva-voce examination and assessment of paper and its presentation. There will be NO external evaluation.

ii) If a candidate fails to secure the minimum marks prescribed for successful completion, he has to re-register by paying the prescribed fee at the beginning of subsequent semester(s). He has to submit a fresh paper towards the end of that semester and appear for evaluation by the committee.

5.4 Project Work:

Every candidate shall be required to submit a dissertation on a topic approved by the Project Review Committee.

i) A Project Review Committee (PRC) shall be constituted for each specialization with Head of the Department / a Senior Faculty as Chairman and two other senior faculty members.

ii) Registration of Project Work: A candidate who has been promoted to 3rd semester shall be eligible to register for the project work.

iii) The eligible candidate can choose his project supervisor and submit the title, objective, abstract and plan of action of the proposed project work to the department for approval by the PRC. The candidate whose proposal is approved by the PRC shall register for the project work. The minimum duration of project work will be 36 weeks from the date of registration.

iv) If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. In case of such changes, the candidate has to register afresh.

v) There shall be three reviews on the progress of the project work by the PRC with an interval of 12 weeks. The candidate needs to submit a report on the progress of his work and present it before the PRC for assessment. The PRC may suggest for an extension of date of submission of dissertation if the progress of work is not satisfactory or absent himself for the review.

vi) A candidate who has passed all the theory, laboratory, seminar and term paper examinations and shown satisfactory progress of project work is permitted to submit the dissertation after 36 weeks from the date of registration.

vii) If a candidate fails to submit the dissertation by the end of the 4th semester, he has to take the permission for an extension by paying the semester(s) tuition fee.

viii) Three copies of the Project Thesis certified by the supervisor shall be submitted to the Department.

ix) Project evaluation and Viva-Voce examination is conducted at the end of 4th semester by a committee consisting of Project Supervisor, senior faculty of the department, HoD and an External Examiner nominated by the Chief Controller of Examinations out of a panel of three examiners suggested by the department.

The following grades are awarded for the project work:

i. Excellent
ii. Very Good
iii. Good
iv. Satisfactory
v. Unsatisfactory

The Grade "unsatisfactory" is treated as Fail. Failed Students should take supplementary examination after making required modifications, if any, in the dissertation with a minimum gap of 8 weeks by paying the required examination fee.

6. Criteria for Passing a Course and Award of Grades:

6.1 Criteria for Passing a Course:

i) A candidate shall be declared to have passed in individual theory / laboratory course, if he secures a minimum of 50% aggregate marks (internal & semester end examination marks put together), subject to securing a minimum of 40% marks in the semester end examination.

ii) The candidate shall be declared to have passed in seminar / term paper viva-voce if he secures 50% marks.

iii) The candidate shall be declared to have successfully completed the project work if he secures a minimum of 'satisfactory' grade in the project evaluation and viva-voce examination.

iv) On passing a course of a program, the student shall earn assigned credits in that course.

6.2 Method of Awarding Letter Grade and Grade Points for a Course:

A letter grade and grade points will be awarded to a student in each course based on his performance, as per the grading system given below.

Theory /Elective /Laboratory /Seminar / Term Paper /Project Dissertation (%)	Grade Points	Letter Grade
≥ 90	10	O (Outstanding
≥ 80 & < 90	9	A+ (Excellent)
≥ 70 & < 80	8	A (Very Good)
≥ 60 & < 70	7	B+ (Good)
≥ 50 & < 60	6	B (Above Average)
< 50	0	F (Fail)

6.3 Calculation of Semester Grade Point Average (SGPA)* for semester:

The performance of each student at the end of the each semester is indicated in terms of SGPA. The SGPA is calculated as given below:

$$\textbf{SGPA} = \frac{\sum(CR \times GP)}{\sum CR} \quad \text{for each semester.}$$

where CR = Credits of a course

GP = Grade Points awarded for a course

* SGPA is calculated for a candidate who passed all the courses in that semester.

6.4 Eligibility for Award of B.Tech Degree:

A student will be declared eligible for the award of the M. Tech. Degree if he fulfills the following academic regulations.

(a) Pursued a course of study for not less than two academic years and not more than four academic years.

(b) Registered for prescribed **70** credits and secured **70** credits.

(c) Students, who fail to complete their Two years Course of study within Four years or fail to acquire the prescribed **70** Credits for the award of the degree within four academic years from the year of their admission shall forfeit their seat in M. Tech course and their admission shall stand cancelled.

6.5 Calculation of Cumulative Grade Point Average (CGPA) for Entire Program:

The CGPA is calculated as given below:

$$\textbf{CGPA} = \frac{\sum(CR \times GP)}{\sum CR} \quad \text{for entire program.}$$

where CR = Credits of a course

GP = Grade points awarded for a course

* CGPA is calculated for a candidate who passed all the prescribed courses excluding project work.

6.6 Award of Division:

After satisfying the requirements prescribed for the completion of the program, the student shall be eligible for the award of B.Tech Degree and shall be placed in one of the following grades:

CGPA	Class
≥ 7.5	First Class with Distinction
≥ 6.5 & < 7.5	First Class
≥ 6.0 & < 6.5	Second Class

7. Supplementary Examinations

i) Supplementary examinations will be conducted once in a year along with regular examinations.

ii) Semester end supplementary examinations shall be conducted till next regulation comes into force for that semester after the conduct of the last set of regular examinations under the present regulation.

iii) Thereafter supplementary examinations will be conducted in the equivalent courses as decided by the Board of Studies concerned.

8. Re-admission Criteria

A candidate, who is detained in a semester due to lack of attendance has to obtain written permission from the Principal for readmission into the same semester after duly fulfilling the required norms stipulated by the college and by paying the required tuition fee and special fee in addition to paying an administrative fee of Rs. 1,000/-

9. Break in Study

Student, who discontinues the studies for what-so-ever reason, can get readmission into appropriate semester of M.Tech program only with the prior permission of the Principal of the College, provided such candidate shall follow the transitory regulations applicable to the batch he joins. An administrative fee of Rs.2,000/- per each year of break in study in addition to the prescribed tuition and special fees shall be paid by the candidate to condone his break in study.

10. Transitory Regulations

A candidate, who is detained or discontinued in a semester, on readmission shall be required to do all the courses in the curriculum prescribed for the batch of students in which the student joins subsequently. However, exemption will be given to those candidates who have already passed such courses in the earlier semester(s) he was originally admitted into and he will be offered substitute subjects in place of them as decided by the Board of Studies. However, the decision of the Board of Studies will be final.

11. Withholding of Results

If the student has not paid the dues, if any, to the College or if any case of indiscipline is pending against him, the result of the student will be withheld. His degree will be withheld in such cases.

12. Malpractices

i) The Principal shall refer the cases of malpractices in internal assessment tests and semester end examinations to a malpractice enquiry committee constituted by him for the purpose. Such committee shall follow the approved levels of punishment. The Principal shall take necessary action against the erring students based on the recommendations of the committee.

ii) Any action by the candidate trying to get undue advantage in the performance or trying to help another, or derive the same through unfair means is punishable according to the provisions contained hereunder.

DISCIPLINARY ACTION FOR MALPRACTICES/IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices / Improper conduct	Punishment
If the candidate		
1.a	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination.)	Expulsion from the examination hall and cancellation of the performance in that subject only.
b	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through Cell phones with any candidates or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester / year. The hall ticket of the candidate shall be cancelled.

3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for the examinations of the remaining subjects of that semester / year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the impostor is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or takes out or arranges to send out the question paper during the examination or answer book during or after the examination.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester / year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of performance in that subject.

6.	Refuses to obey the orders of the Chief Superintendent/Assistant Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in or around the examination hall or organises a walkout or instigates others to walkout or threatens the officer-in-charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the Officer-in-charge or any person on duty in or outside the examination hall of any of his relations or indulges in any other act of misconduct or mischief which results in damage to or destruction of property in the examination hall or any part of the college campus or engages in any other act which in the opinion of the Officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	Expulsion from the examination hall and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester / year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The candidate is also debarred for two consecutive semesters from class work and all university examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The candidate is also debarred and forfeits the seat.

9	If student of the college who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the college will be handed over to the police and a police case is registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester / year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester / year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be referred to the Chief Superintendent of Examinations for future action towards suitable punishment.	

iii) The involvement of the staff, who are in charge of conducting examinations, valuing examination papers and preparing / keeping records of documents related to the examinations in such acts (inclusive of providing incorrect or misleading information) that infringe upon the course of natural justice to one and all concerned at the examination shall be viewed seriously and appropriate disciplinary action will be taken after thorough enquiry.

13. Other Matters

i) Deserving physically challenged candidates will be given additional examination time and a scribe based on the certificate issued by the concerned authority. Students who are suffering from contagious diseases are not allowed to appear either for internal or semester end examinations.

ii) The students who participated in coaching / tournaments held at State / National / International levels through University / Indian Olympic Association during semester end external examination period will be promoted to subsequent semesters as per the guidelines of University Grants Commission Letter No. F.1-5/88 (SPE/PES), dated 18-08-1994.

iii) The Principal shall deal in an appropriate manner with any academic problem which is not covered under these rules and regulations, in consultation with the Heads of the Departments and subsequently such actions shall be placed before the Academic Council for ratification. Any emergency modification of regulation, approved in the meetings of the Heads of the Departments shall be reported to the Academic Council for ratification.

17. General

i) The Academic Council may, from time to time, revise, amend or change the regulations, schemes of examination and /or syllabi.

ii) The academic regulations should be read as a whole for the purpose of any interpretation.

iii) In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman of the Academic Council is final.

v) Wherever the word he, him or his occurs, it will also include she, her and hers.

VI. CURRICULAR COMPONENTS

Sl. No.	Course Work - Subject Areas	Total No.of Credits	% of Total Credits
1	Baisc Sciences (BS)	3	4.28
2	Humanities and Social Sciences (HSS)	3	4.28
3	Professional Core (PC)	25	35.72
4	Professional Electives (PE)	9	12.86
7	Others (Seminar, Term Paper, Dissertation, etc.)	30	42.86

COURSE STRUCTURE

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SYLLABUS

COURSE STRUCTURE

I Semester

Sl. No.	Course Code	Name of the Course / Laboratory	No.of Periods per week			No.of Credits
			L	T	P	
1	MA2902	Linear and Non-Linear Optimization Techniques	4	-	-	3
2	EC2903	Principles of Diital Design Using FPGA**	3	-	2	3
3	EC2904	Advanced Digital Signal Processing	4	-	-	3
4	EC2905	Advanced Microcontrollers	4	-	-	3
5	EC2906	Embedded C	4	-	-	3
6		Professional Elective - I	4	-	-	3
7	EC2910	Advanced Digital Design Lab	-	-	4	2
		Total	**23**	**-**	**6**	**20**

II Semester

Sl. No.	Course Code	Name of the Course / Laboratory	No.of Periods per week			No.of Credits
			L	T	P	
1		Research Methodology	4	-	-	3
2	EC2911	Advanced Embedded Systems **	3	-	2	3
3	EC2912	Principles of CMOS Analog Design	4	-	-	3
4	EC2913	Internet of Things	4	-	-	3
5		Professional Elective - II	4	-	-	3
6		Professional Elective - III	4	-	-	3
7	EC2920	Embedded Systems Lab	-	-	4	2
8		Seminar	-	-	-	2
		Total	**23**	**-**	**6**	**22**

** Project Based Theory Course

L : Lecture **T : Tutorial** **P : Practical**

III Semester

Sl. No.	Course Code	Name of the Course / Laboratory	No.of Periods per week			No.of Credits
			L	T	P	
1		Term Paper	-	-	4	2
2		Dissertation (Initiated in third semester)	-	-	-	-
		Total	**-**	**-**	**4**	**2**

IV Semester

Sl. No.	Course Code	Name of the Course / Laboratory	No.of Periods per week			No.of Credits
			L	T	P	
1		Dissertation (Carried out in third & Fourth Semester)	-	-	52	34
		Total	**-**	**-**	**52**	**34**

Professional Electives:

Professional Elective - I

EC2907 Embedded Networking

EV2908 Sensors and Actuators

EE2909 Low Power CMOS Digital Design

Professional Elective - II

EC2914 SoC Design

EC2915 Embedded Real Time Operating Systems

EC2916 Embedded System Design

Professional Elective - III

EC2917 Advanced Computer Networks

EC2918 Hardware Software Co-Design

EC2919 Wireless Sensor Networks

SYLLABUS

LINEAR AND NON-LINEAR OPTIMIZATION TECHNIQUES

I Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course objectives

To make the students

- familiarize different optimization techniques and approaches.
- provide the concepts of various classical and modern methods of constrained and constrained problems in both single and multivariable
- understand Non – Linear optimization problems.
- know evolutionary optimization methods

Learning Outcomes

Upon successful completion of the course, the students will be able to

- apply the knowledge of Mathematics in analyzing on engineering problems.
- formulate optimization problem
- develop an optimization problem in standard form and asses the optimality of a solution.
- solve various constrained and unconstrained problems in single variable as well as multi variable.
- apply the concepts of optimality criteria for various types of optimization problems.

Course Content

Unit-I: Linear Optimization

Formulation of LPP, graphical solution, standard form of linear programming problem, simplex method, big-M method.

Unit-II: Classical Optimization Techniques

Introduction-single-variable optimization-multivariable optimization, nonlinear programming: one-dimensional minimization methods **:** introduction –unimodal function –elimination methods: unrestricted search - exhaustive search-dichotomous search - interval halving method- fibonacci method - golden section method.

Unit-III: Nonlinear Programming I: Unconstrained Optimization Techniques

Introduction –direct search methods: random search methods-univariate method-pattern directions- Powell's method- indirect search (descent) methods: gradient of a function -steepest descent (Cauchy) method - conjugate gradient (Fletcher–Reeves) method.

Unit-IV: Nonlinear Programming II: Constrained Optimization Techniques

Optimization with equally and inequality constraints, direct methods, indirect methods using penalty functions, lagrange multipliers, geometric programming.

Unit- V: Modern Methods of Optimization

Genetic algorithms: introduction – representation of design variables, representation of objective function and constraints, genetic operators - ant colony optimization: introduction, basic concepts, ant searching behavior, path retracing and pheromone updating, pheromone trail evaporation algorithm.

Text Books:

1. Singiresu S.Rao, "Engineering Optimization, Theory and Practice", New Age International (P) Limited Publishers. 4th edition. (Units- I to V)
2. Kalyan moy Deb, "Optimization for Engineering Design", PHI, Delhi, 2014.

References:

1. S.D. Sharma, "Operations Research", Kedarnath Publishers,8th edition, 2007.
2. E.J. Haug and J. S. Arora, "Applied Optimal Design", Wiley, New York.
3. Marco Dorigo and Thomas stutzle, "Ant colony optimization", MIT press, 2004.
4. S.N.Sivanandan, S.N. Deepa, "Introduction to genetic Algorithms", Springer.

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PRINCIPLES OF DIGITAL DESIGN USING FPGA

I Semester

Lecture	: 3	Practical	: 2	Internal Marks	: 40
Credits	: 3			External Marks	: 60

Course objectives

To make the students

- familiarize with design steps and various families of FPGA architecture.
- explore the design of digital circuits using FPGAs.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- identify FPGA architectures and resources.
- select suitable device family of FPGA for a given application.
- implement various digital logic circuits using FPGAs.

Course Content

UNIT-I: Introduction

Overview, design methodologies, why FPGAs, design flow, verification and testing, design implementation (CAD) tools.

UNIT-II: Field Programmable Gate Arrays

Introduction, programming technology, device architecture- Xilinx logic cell array, - Xilinx 2000, 3000, 4000, general features of Virtex device family FPGAs; Actel ACT device architecture-ACT1, ACT2, ACT3, technology trends.

UNIT-III: Finite State Machines

Introduction, finite state machines, state transition table, state assignment for FPGAs, hazard and one-hot encoding.

UNIT-IV: Placement and Routing

Introduction, placement and routing- min-cut placement, iterative improvement, simulated annealing, segment channel routing and maze routing, routability and routing resources, net delays.

UNIT-V: Design Guidelines and Case Studies

Introduction, combinational circuits-parallel adder, sequential circuits- decade counter, asynchronous inputs, static RAM tester, pseudorandom number generation.

Text Books:

1. Pak.K.Chan, Samiha Mourad, Digital Design Using Field Programmable Gate Arrays, Pearson Education,1994. (UNITS-I,III,IV,V)
2. Stephen M. Trimberger, Field-Programmable Gate Array Technology, Springer,2007. (UNIT-II)

References:

1. John V. Oldfield, Richard C. Dorf (1995), Field-Programmable Gate Arrays, Wiley.
2. Ian Grout (2009), Digital Systems Design With FPGAs and CPLDs, Newness.
3. https://www.xilinx.com/support/documentation/data_sheets/3000.pdf.
4. https://www.xilinx.com/support/documentation/data_sheets/4000.pdf.
5. https://www.xilinx.com/support/documentation/data_sheets/ds031.pdf.
6. https://www.xilinx.com/support/documentation/data_sheets/ds112.pdf.

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ADVANCED DIGITAL SIGNAL PROCESSING

I Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course objectives

To make the students

- familiarize with concepts of different types of filter banks and structures.
- familiarize with different adaptive algorithms and its applications on various fields.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- understand the fundamentals of multirate signal processing and its applications.
- design perfect reconstruction filter bank system
- understand the fundamentals of adaptive systems and its applications.

Course Content

Unit-I: Basic Multirate Operations

Decimation and interpolation, time-domain characterization, frequency-domain characterization, cascade equivalences, filters in sampling rate alteration systems, polyphase decomposition.

Unit-II: Filter Banks

Digital filter banks- uniform DFT filter banks, polyphase implementation of uniform filter banks, nyquist filters. two channel Quadrature-Mirror Filter (QMF) bank-filter bank structure, analysis of two channel QMF bank, alias free filter bank, alias free realization, alias free FIR QMF bank, alias free IIR QMF bank, perfect reconstruction two channel QMF bank.

Unit-III: Adaptive Systems

Adaptive systems- definitions and characteristics- properties, adaptive linear combiner-input signal and weight vectors - performance function-gradient and minimum mean square error.

Unit-IV: Adaptive Algorithms

Searching performance surface-stability and rate of convergence - learning curve-gradient search - Newton's method - method of steepest descent – comparison. LMS algorithm- convergence of weight vector. The LMS/Newton algorithm.

Unit-V: Applications of Adaptive Systems

Applications-adaptive modeling and system identification-adaptive modeling for multipath communication channel, geophysical exploration, FIR digital filter synthesis.

Text Books:

1. Sanjit K. Mitra, " Digital Signal Processing: A computer based approach", McGraw Hill, 1998. (Units – I&II)
2. Bernard Widrow and Samuel D. Stearns, "Adaptive Signal Processing", Pearson Education, 2005. (Units – III,IV& V).

Reference Books:

1. P.P. Vaidyanathan, "Multirate Systems and Filter Banks." Prentice Hall. PTR. 1993.
2. Simon Haykin, "Adaptive Filter Theory", Pearson Education, 2003.
3. J.G. Proakis. D.G. Manolakis. "Digital Signal Processing: Principles. Algorithms and Applications", 3rd Edn. Prentice Hall India, 1999.
4. N.J. Fliege. "Multirate Digital Signal Processing " John Wiley 1994.

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ADVANCED MICROCONTROLLERS

I Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

To make the students

- familiarize with architecture and the instruction set of different microcontrollers.
- familiarize with assembly language programming of various microcontrollers.

Learning Outcomes:

Upon successful completion of the course, the students will be able to

- understand the internal architecture of Atmel, PIC and ARM microcontrollers.
- understand ARM architecture support for high level languages, system level development and operating systems.
- apply knowledge of soft skills and other resources for system level development.
- discriminate the performance of different microcontrollers.

Course Content

UNIT - I: Atmel Microcontrollers

Introduction to Atmel microcontrollers (89CXX and 89C20XX), architectural overview and pin description of 89C51 and 89C2051, precision analog comparator in 89C2051, ADC using precision analog comparator, power saving options, pulse generation, PWM, pulse width measurement and frequency counter.

UNIT - II: PIC Microcontrollers

Overview and features, PIC 16C6X/7X: architecture, addressing modes, instruction set, memory organization, I/O ports, interrupts, timers, ADC. PIC 16F8XX: pin diagram, program memory, data memory, Interrupts, I/O ports and timers. CCP module in PIC 16F877, MSSP module, USART.

UNIT - III: ARM Processors

Introduction, architecture, assembly language programming, ARM organization and implementation, instruction set, thumb instruction set, architectural support for high level languages.

UNIT - IV: ARM Architectural Support for System Development

The ARM memory interface, memory hierarchy, the Advanced Microcontroller Bus Architecture (AMBA), the ARM reference peripheral specification, hardware system prototyping tools, the ARMulator, the JTAG boundary scan test architecture, the ARM debug architecture, embedded trace, signal processing support.

UNIT - V: Architectural Support for Operating Systems

Introduction to operating systems, ARM system control coprocessor, CP15 protection unit registers, ARM protection unit, CP15 MMU registers, ARM MMU architecture, synchronization, context switching.

Text Books:

1. Ajay V Deshmukh, "Microcontrollers-Theory and Applications", TMH Publications,1st Edition,2005 (Unit-I, II).
2. Stephen B Furber , "ARM system on chip Architecture", Pearson Publications, 2nd Edition. (Unit-III, IV,V).

References:

1. M. Ali Mazidi and J. Gillispie Mazidi , "The 8051 Microcontroller and Embedded Systems Using Assembly and C", 2nd Edition.
2. Lucio Bi Jasio, "PIC Microcontrollers", Newnes Publishers, 1st Edition, 2008.

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EMBEDDED C

I Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course objectives

To make the students

- understand the basic concepts of embedded systems, processors, and programming languages.
- familiarize with various interfaces, memory, and power consumption.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- distinguish C and Embedded C.
- select the processor, memory and operating system for an application.
- design and develop an application using Embedded C.

Course Content

UNIT - I: Programming Embedded Systems in C

Introduction to embedded system, selection: processor, programming language and operating system; steps in developing embedded software.

External interface of the standard 8051, reset requirements, clock frequency and performance, memory issues, I/O pins, timers, interrupts, serial interface, power consumption

UNIT - II: I/O Port Programming

Basic techniques for reading from port pins, reading and writing bytes, reading and writing bits (simple version), reading and writing bits (generic version), need for pull-up resistors, dealing with switch bounce, reading switch inputs (basic code), example: counting goats.

UNIT - III: Object Oriented Concepts

Object-oriented programming with C, the project header (MAIN.H), the port header (PORT.H), restructuring the goat-counting example.

UNIT - IV: Real-time Constraints

Introduction, creating 'hardware delays' using timer 0 and timer 1, generating a precise 50 ms delay, creating a portable hardware delay, use of timer 2, need for

'timeout' mechanism, creating loop timeouts, testing loop timeouts, reliable switch interface, creating hardware timeouts, testing a hardware timeout.

UNIT - V: Applications

Timer program, keyboard scanner, serial port programming, LCD programming.

Text Books:

1. Michael J. Pont, "Embedded C", Pearson Education, 2nd Edition, 2008.(Units I-IV)
2. Zdravko Karakehayov, Knud Smed Christensen, Ole Winther, "Embedded Systems Design with 8051 Microcontrollers", Marcel Dekker, Special Indian Edition,2010.(Unit V)

Reference Books:

1. Muhammad Ali Mazidi, Janice Gillispie Mazidi, Rolin D. McKinlay, "The 8051 Microcontroller and Embedded Systems", Pearson Education, 2nd Edition, 2008.
2. Michael Barr, "Programming Embedded Systems in C and C++", Oreilly, 2003.

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Professional Elective - I

EMBEDDED NETWORKING

I Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives

To make the students

- know the concepts of SPI, I^2C and CAN Interfaces.
- familiarize with networking basics and security.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- understand the principles of SPI, I^2C, and CAN Interfaces.
- understand the basic concepts of networking and security.

Course Content

UNIT – I: SPI and I^2C Interface

Serial peripheral interface: introduction, SPI mode, SPI C library functions, applications of SPI.

Inter-Integrated Circuit: the I^2C Protocol, PIC18 MSSP module in I^2C mode, registers for I^2C operation, PIC18 I^2C master and slave mode.

UNIT – II: CAN Principles

Overview of Controller Area Network, CAN messages, error handling, fault confinement, CAN message bit timing, synchronization issue, PIC18 CAN module, CAN modes of operation, CAN module registers, CAN module functional modes.

UNIT – III: CAN Transmission and Reception

CAN message buffers, CAN message transmission, message reception, message acceptance filters and masks, baud rate setting and timing parameters, physical CAN bus connection.

UNIT – IV: Networking Basics

Sockets, TCP/IP networking, Ethernet, Wi-Fi and IEEE 802.11, Bluetooth.

UNIT – V: Platform and Content Security

Principles, concepts and building blocks, platform support for security.

Text Books:

1. Han-Way Huang, "PIC Microcontroller: An Introduction to Software and Hardware Interfacing", Thomson publishers. (Units: I,II&III).
2. Peter Barry and Patrick Crowley, "Modern Embedded Computing", 1st Edition, Elsevier/Morgan Kaufmann, 2012. (Units: IV&V)

Reference Books:

1. Frank Vahid, Givargis, "Embedded Systems Design: A Unified Hardware/Software Introduction", Wiley Publications.
2. Jan Axelson, "Parallel Port Complete", Penram publications.
3. Dogan Ibrahim, "Advanced PIC Microcontroller Projects in C", Elsevier Publishers, 2008.
4. Glaf P.Feiffer, Andrew Ayre and Christian Keyold, "Embedded Networking with CAN and CAN open", Embedded System Academy 2005.

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Professional Elective - I

SENSORS AND ACTUATORS

I Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives

To make the students

- familiarize with various types of sensors and actuators.
- understand the concepts of smart sensors.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- understand the principles of different sensors and actuators.
- use sensors in practical applications.

Course Content

UNIT - I: Introduction to Systems

Measurement systems, control systems, microprocessor based controllers, data loggers, single and multichannel data acquisition systems, sensor based data acquisition systems, electro mechanical A/D converter, digital transducer.

UNIT - II: Mechanical and Electromechanical Sensors

Selection of a sensor, acoustic temperature sensor, dielectric constant and refractive index thermo sensors ,thermometer – resistance change type thermometric sensors, thermo emf sensors, thermal radiation sensors, quartz crystal thermoelectric sensors, heat flux sensors, force/stress sensors using quartz resonators, pyrometers, ultrasonic sensors.

UNIT - III: Magnetic Sensors

Introduction, principles, Hall effect sensors, eddy current sensors, angular/rotary movement transducers – synchros – synchro-resolvers, electromagnetic flow meters, switching magnetic sensors, SQUID sensor.

UNIT - IV: Smart Sensors

Introduction, primary sensors, excitation, amplification, filters, converters, compensation, information coding processing, data communication, the automation. Sensors applications: Introduction, on-board automobile (automotive) sensors, home appliance sensors.

UNIT – V: Actuators

Actuation systems, pneumatic and hydraulic systems, directional control valves, pressure control valves, cylinders, process control valves, rotary actuators.

Mechanical actuation systems: Types of motion, kinematic chains, cams, gears, ratchet and pawl, belt and chain drives, bearings.

Text Books:

1. D. Patranabis, "Sensors and Transducers", PHI Learning Private Limited, 2nd Edition, 2006. (Units: II, III, IV)
2. W. Bolton, "Mechatronics", Pearson Education Limited, 3rd Edition, 2003. (Units: I, V)

Reference Books:

1. D. Patranabis, "Sensors and Actuators", PHI, 2nd Edition, 2013.
2. H..S.kalsi, "Electronic Instrumentation", TMH, 3rd Edition,2012.

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Professional Elective - I

LOW POWER CMOS DIGITAL DESIGN

I Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

To make the students

- familiarize with the limits of power and sources of power consumption in CMOS digital circuits.
- understand various approaches for minimizing power consumption.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- understand the various sources of power consumption in CMOS digital circuits.
- understand the techniques for minimizing power consumption.
- identify various methodologies for the design of low power circuits.

Course Content

UNIT-I : Limits of Power and Sources of Power Consumption

Introduction, background, theoretical limits, quasi-adiabatic microelectronics, practical limits, switching component of power, short-circuit component of power, leakage component of power, static power.

UNIT-II : Voltage Scaling Approaches

Reliability-driven voltage scaling, technology-driven voltage scaling, energy x delay minimum based voltage scaling, voltage scaling through optimal transistor sizing, voltage scaling using threshold reduction, architecture-driven voltage scaling.

UNIT-III : Adiabatic Switching

Adiabatic charging, adiabatic amplification, adiabatic logic gates, stepwise charging, pulsed-power supplies.

UNIT-IV : Minimizing Switched Capacitance

Algorithmic optimization, architecture optimization, logic optimization, circuit optimization, physical design.

UNIT-V : Low Power Design Methodology

Low power physical design, low power gate-level design, low power architecture-level design, algorithmic-level power reduction, power estimation techniques.

Text Books :

1. Anantha P. Chandrakasan and Robert W. Brodersen, "Low Power Digital CMOS Design", Springer Science, 1st Edition, 1995 (Units I-IV).
2. Abdellatif Bellaouar and Mohamed Elmasry, "Low-power Digital VLSI design : Circuits and Systems", Springer Science, 1st Edition, 1995 (Unit V).

Reference Books:

1. Jan M. Rabaey and Massoud Pedram, "Low Power Design Methodologies", Springer International Series, 1st Edition, 1996.
2. Jan Rabaey, " Low Power Design Essentials", Springer US, 2009.

Gary K. Yeap, "Practical Low Power Digital VLSI Design", Springer, 1998.

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ADVANCED DIGITAL DESIGN LAB

I Semester

Practical	: 4	Internal Marks	: 40
Credits	: 2	External Marks	: 60

Course Objectives

To make the students

- familiarize with the design and implementation of various digital systems.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- design digital circuits
- implement various combinational and sequential circuits in FPGA.
- perform power and delay analysis on the designed circuits in back-end environment.

List of Experiments:

- For Part-1, develop the program in HDL, perform simulation, synthesis and implement in FPGA.
- For Part-2, perform transistor level circuit realization and simulation.

Note: Any four from a to f of part-1and any three from a to d of part-2 to be performed.

i) Part-1:

a) Serial and parallel data transfer systems.
b) Digital display decoder systems.
c) Adder/subtractor module.
d) Barrel shifter module.
e) Dual port RAM module.
f) ALU.
g) Design of ASIP– Open ended experiment.

ii) Part-2:

a) Basic Logic gates
b) Full Adder.
c) Multiplexer.
d) Data flip-flop/register.

References:

1. Leo Chartrand, “Advanced Digital Systems: Experiments and Concepts with CPLDs”, Thomson Delmar Learning, 2005.
2. R. Jacob Baker, “CMOS: Circuit Design, Layout, and Simulation”, IEEE Press, Wiley, 2010.

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RESEARCH METHODOLOGIES

II Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives

To make the students

- familiarize the objectives, motivation and significance of research.
- know research methodologies.
- define research problem and perform data analysis.
- write a research paper and report.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- understand research approaches
- understand various research methodologies
- define a research problem
- perform data analysis
- write research papers and reports

Course Content

UNIT – I: Introduction

Introduction, objectives and motivation of research, types of research, research approaches, significance of research methods.

UNIT – II: Research Methodology

Research methods versus methodology, research and scientific method, importance of knowing how research is done, research process. criteria for good research.

UNIT – III: Defining Research Problem

The research problems, necessity of defining the problem, technique involved in defining a problem, review of related literature, purpose of literature survey, identifying the current status, presentation of literature survey findings. critique, survey and peer review process.

UNIT – IV: Research Design and Data Analysis

Meaning of research design, features of good design, important concepts relating to research design, different research designs, basic principles of experimental designs.

Methods of data collection - collection of primary data, observation method, interview method, collection of data through questionnaires, collection of data through schedules, difference between questionnaires and schedules, some other methods of data collection, collection of secondary data, selection of appropriate method for data collection, case study method.

Processing and analysis of data **-** processing operations, some problems in processing, elements, types of analysis, statistics in research.

UNIT – V: Research Paper and Report Writing

Final paper presentation. significance of report writing, different steps in writing report, layout of the research report, types of report, precautions for writing research reports.

Text Books:

1. C.R.Kothari, “Research Methodology Methods and Techniques”, Wishwa Prakashan Publishers,Second Edition.

Reference Books:

1.Template of ASCE/ASME/IEEE for paper writing.

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ADVANCED EMBEDDED SYSTEMS

II Semester

Lecture	: 3	Practical	: 2	Internal Marks	: 40
Credits	: 3			External Marks	: 60

Course Objectives

To make the students

- familiarize with advanced embedded systems.
- familiarize with computing aspects, optimization techniques used in advanced embedded systems.

Learning Outcomes:

Upon successful completion of the course, the students will be able to

- know the characteristics of advanced embedded systems.
- understand the concepts of embedded computing.
- demonstrate the architecture of Intel atom processor.

Course Content

UNIT-I: Attributes and Future of Embedded System

Embedded platform characteristics: Central Processing Unit (CPU), integration level, power consumption, form factor, expansion, application-specific hardware, certification, reliability/availability, user interfaces, connectivity, security

The future of embedded systems: Technology trends, connectivity, storage, sensing; issues, applications, and initiatives: energy, security, health, challenges and uncertainties: open systems, internet access, and neutrality, privacy, successful commercialization

UNIT-II: Embedded Computing

Complex systems and microprocessors, embedded system design process, CPUs-CPU performance, CPU power consumption.

UNIT-III: Program Design and Analysis

Program optimization, program-level performance analysis, software performance optimization, program-level energy and power analysis and optimization, analysis and optimization of program size, program validation and testing

UNIT-IV: Power Optimization and parallel Processing

Basics, power profile of an embedded computing system, constant versus dynamic power, simple model of power efficiency, advanced configuration and power interface,

optimizing software for power performance, types and levels of parallelism, classification of parallel architectures, basic parallel techniques.

UNIT-V: Architecture of Intel E6XX Processor

Intel Atom E6XX series platforms, multi-radio communications design, multimedia design, modular references.

Text Books:

1. Wayne Wolf, "Computers as Components: Principles of Embedded Computer Systems Design", Morgan Kaufman Publishers, 2004. (UNITS II & III).
2. Peter Barry and Patrick Crowley, "Modern Embedded Computing", 1st Edition, Elsevier/Morgan Kaufmann, 2012. (UNITS I, IV & V)

Reference Books:

1. DezsoSima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architectures", Pearson Education Ltd.
2. Tammy Noergaard, "Embedded Systems Architecture", Newnes, 2005.
3. Joseph A. Fisher, Paolo Faraboschi and Cliff Young , "Embedded Computing – A VLIW Approach to Architecture, Compilers and Tools", Elsevier/Morgan Kaufmann, 2005

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PRINCIPLES OF CMOS ANALOG DESIGN

II Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives

To make the students

- familiarize with the MOS transistor operation and its models
- understand the operation of various analog circuits.
- familiarize with types of noise in circuit elements and noise models.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- understand the operation and modelling of MOS transistor.
- understand the operation of current mirrors, single-stage amplifiers, opamps, and switched capacitor circuits.
- understand the compensation of opamps.
- model the noise components in circuit elements and analyze them in various circuits.

Course Content

UNIT-I : MOS transistors operation and modelling

Symbols for MOS transistors, basic operation, large-signal modelling , body effect, p-channel transistors, low- and high-frequency small-signal modelling in the active region, small-signal modelling in the triode and cutoff regions, analog figures of merit and trade-offs, advanced MOS modelling - subthreshold operation, mobility degradation, parasitic resistances, short-channel effects, leakage currents.

UNIT-II : Basic current mirrors and single-stage amplifiers

Simple CMOS current mirror, common-source amplifier, source-follower or common-drain amplifier, common-gate amplifier, source-degenerated current mirrors, cascode current mirrors, cascode gain stage, MOS differential pair and gain stage.

UNIT-III : Basic opamp design and compensation

Two-stage CMOS opamp - opamp gain, frequency response, slew rate, n-channel orp-channel input stage, systematic offset voltage; opamp compensation - dominant-pole compensation and lead compensation, compensating the two-stage

opamp, making compensation independent of process and temperature; folded-cascode opamp - small-signal analysis, slew rate; fully differential opamps - fully differential folded-cascode opamp, alternative fully differential opamps, low supply voltage opamps.

UNIT-IV : Noise, linearity analysis and modelling

Time-domain analysis - root mean square (rms) value, SNR, units of dbm, noise summation; frequency-domain analysis - noise spectral density, white noise, 1/f, or flicker, noise, filtered noise, noise bandwidth, piecewise integration of noise, 1/f noise tangent principle; Noise models for circuit elements – resistors, diodes, bipolar transistors, MOSFETs, opamps, capacitors and inductors, sampled signal noise, input-referred noise noise analysis examples - opamp example, CMOS differential pair example, fiber-optic transimpedance amplifier example; dynamic range performance - total harmonic distortion (THD), third-order intercept point (IP3), spurious-free dynamic range (SFDR), signal-to-noise and distortion ratio (SNDR).

UNIT-V : Switched capacitor circuits

Switched capacitor circuits : Basic building blocks – opamps, capacitors, switches, non-overlapping clocks; basic operation and analysis - resistor equivalence of a switched capacitor, parasitic-sensitive integrator, parasitic-insensitive integrators, signal-flow-graph analysis; noise in switched-capacitor circuits; first-order filters - switch sharing, fully differential filters; biquad filters - low-Q and high-Q biquad filter; charge injection, switched-capacitor gain circuits - parallel resistor-capacitor circuit, resettable gain circuit, capacitive-reset gain circuit, correlated double-sampling techniques.

Text Books :

1. Tony Chan Carusone, David A. Johns, Kenneth W. Martin, “Analog Integrated Circuit Design”, John Wiley & Sons, 2nd Edition, 2012.

Reference Books :

1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewls, Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits”, John Wiley & Sons, 4th Edition, 2001.
2. Behzad Razavi’ “ Design of Analog CMOS Integrated Circuits”, McGraw-Hill International Edition, 2001.

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INTERNET OF THINGS

II Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives

To make the students

- undestand the concepts of M2M to IoT.
- familiarize with data and knowledge management and usage of devices in IoT technology.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- understand the concepts of M2M to IoT.
- use devices, gateways and data management in IoT.
- apply IoT in industrial and commercial building automation.

Course Content

UNIT-I: M2M to IoT

The vision-introduction, from M2M to IoT, M2M towards IoT-the global context, a use case example, differing characteristics.

UNIT-II: M2M to IoT – A Market Perspective

Introduction, some definitions, M2M value chains, IoT value chains, an emerging industrial structure for IoT, the international driven global value chain and global information monopolies. **M2M to IoT-An Architectural Overview–** Building an architecture, main design principles and needed capabilities, An IoT architecture outline, standards considerations.

UNIT-III: M2M and IoT Technology Fundamentals

Devices and gateways, Local and Wide Area Networking, data management, business processes in IoT, everything as a service(XaaS), M2M and IoT analytics, knowledge management.

UNIT-IV: IoT Architecture

State of the Art- Introduction, state of the art, **Architecture reference model-** introduction, reference model and architecture, IoT reference model, **IoT reference architecture-** introduction, functional view, information view, deployment and operational view, other relevant architectural views.

UNIT-V: Real World Design and IoT Applications

Real-World Design Constraints- introduction, technical design constraints-hardware is popular again, data representation and visualization, Interaction and remote control. **Industrial Automation-** service-oriented architecture-based device integration. **Commercial Building Automation-** Introduction, case study: phase one-commercial building automation today, case study: phase two- commercial building automation in the future.

Text Books:

1. Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos, David Boyle, "From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence", 1st Edition, Academic Press, 2014.

Reference Books:

1. Rajkamal, "Internet of Things: Architecture, Design Principles And Applications", McGraw Hill Higher Education
2. Vijay Madisetti and Arshdeep Bahga, "Internet of Things (A Hands-on-Approach)", 1stEdition, VPT, 2014.
3. Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach to Connecting Everything", 1st Edition, Academic press Publications, 2013

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Professional Elective - II

SOC DESIGN

II Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives

To make the students

- understand the concepts of System-On-Chip design technology.
- introduce components in a typical SoC system.
- familiarize with the concept of different processor cores.

Course Outcomes:

Upon successful completion of the course, the students will be able to

- understand architecture, design issues, core libraries and EDA tools required for SoC design.
- understand design methodology for logic cores, soft and hard cores, memory and analog cores.
- perform SoC design validation, prototyping and verification.

UNIT - I: Introduction to Architecture Designs

Architecture and design issues of SoC, hardware software co-design, co-design flow, core libraries, EDA tools and web pointers.

UNIT - II: Design Methodology for Logic Cores, Soft and Firm Cores

Logic Cores: SoC design flow, guidelines for design reuse and physical design.

Soft and Firm Cores: Soft core design flow, design process for hard cores, sign-off checklist, deliverables and system integration.

UNIT - III: Design methodology for Memory Cores and Analog Cores

Memory Cores: Embedded memories and design methodology, specifications of analog circuits, circuit techniques, memory compiler, simulation models.

Analog Cores: Analog-to-digital converter, digital-to-analog converter, phase-locked loops, high speed circuits

UNIT - IV: Design Validation

Core-level validation, core validation plan, test benches, core-level timing verification, core interface verification, protocol verification, gate-level simulation, SoC design validation, co-simulation, emulation, hardware prototypes.

UNIT - V: Core Design Examples

Micro processor cores, V830 R/AV super scalar RISC core, design of power PC 603e G2 core, memory core generators, core integration and on-chip bus.

Text Books:

1. Rochit Raj Suman, "System-on-a-chip: Design and Test", Artech House, 2000.

Reference Books:

1. Jason Andrews – Newness "Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) ", BK and CDROM.
2. Prakash Rashinkar, Peter Paterson and Leena Singh L "System on Chip Verification – Methodologies and Techniques", Kluwer Academic Publishers, 2001.
3. Ricardo Reis,"Design of System on a Chip: Devices and Components", 1st Ed., Springer 2004.

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Professional Elective - II

EMBEDDED REAL TIME OPERATING SYSTEMS

II Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives

To make the students

- introduce the basic concepts and applications of real time operating systems.
- familiarize with the basic concepts and programming of Unix/Linux and RT Linux.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- understand the concepts of real time operating systems.
- develop software for embedded systems.
- develop the hardware and software architectures for digital camera application.

Course Content

UNIT – I: Introduction to Real Time Operating System

OS services, process management, timer functions, event functions, memory management, device, file and IO systems management, interrupt routines in RTOS environment and handling of interrupt source calls, Real-Time Operating Systems, basic design using an RTOS, RTOS task scheduling models, interrupt latency and response of the tasks as performance metrics, OS security issues.

UNIT – II: Real Time Operating Systems for Embedded systems.

Basic functions and types of RTOS for embedded systems - µCOS-II, VxWorks, Windows CE, OSEK.

UNIT – III: Case Study-Program Modeling with RTOS

Case study - digital camera hardware and software architecture, coding for sending application layer byte streams on a TCP/IP network using RTOS VxWorks.

UNIT – IV: Target Image Creation

Off-the-shelf operating systems, operating system software, target image creation for Windows XP embedded, porting RTOS on a microcontroller based development board.

UNIT – V: Programming in Linux and RTLINUX

Overview and programming concepts of Unix/Linux, shell programming, system programming – fork demo, semaphores. Overview of RT Linux, core RT Linux API, program to display a message periodically, semaphore management.

Text Books:

1. Rajkamal, "Embedded Systems-Architecture, Programming and Design", Tata McGraw Hill Publications, Second Edition, 2008 (units: I,II & III).
2. Dr. K.V.K.K. Prasad, "Embedded/Real-Time Systems" Dream Tech Publications, (units: IV & V).

Reference Books:

1. Labrosse, "Embedding system building blocks ", CMP publishers.
2. Rob Williams," Real time Systems Development", Butterworth Heinemann Publication.

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Professional Elective - II

EMBEDDED SYSTEM DESIGN

II Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives

To make the students

- To introduce the concepts of embedded system hardware and software.
- To familiarize with embedded system design and development.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- understand the concepts of embedded system.
- identify hardware and software requirements for an embedded system.
- design an embedded system.

Course Content

UNIT-I: Introduction

An embedded system-definition, examples, current technologies, integration in system design, embedded system design flow, hardware design concepts, software development, processor in an embedded system and other hardware units, introduction to processor based embedded system design concepts.

UNIT-II: Embedded Hardware

Embedded hardware building blocks, embedded processors – ISA architecture models, internal processor design, processor performance, board memory – ROM, RAM, auxiliary memory, memory management of external memory, board memory and performance. embedded board input / output – serial versus parallel I/O, interfacing the I/O components, I/O components and performance, board buses – bus arbitration and timing, integrating the bus with other board components, bus performance.

UNIT-III: Embedded Software

Device drivers, device drivers for interrupt-handling, memory device drivers, on-board bus device drivers, board I/O drivers, explanation about above drivers with suitable examples. Embedded operating systems –Multitasking and process management, memory management, I/O and file system management, OS

standards example – POSIX, OS performance guidelines, board support packages, middleware and application software – middle ware, middleware examples, application layer software examples.

UNIT-IV: Embedded System Design and Development

Embedded system design and development lifecycle model, creating an embedded system architecture, introduction to embedded software development process and tools- host and target machines, linking and locating software, getting embedded software into the target system, issues in hardware-software design and co-design.

UNIT-V: Embedded System Design implementation and Case Study

Implementing the design-the main software utility tool, CAD and the hardware, translation tools, debugging tools, testing on host machine, simulators, laboratory tools, system boot-up. case study - processor design approach of an embedded system –power PC processor based and micro blaze processor based embedded system design on Xilinx platform

Text Books:

1. Tammy Noergaard "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier(Singapore) Pvt. Ltd. Publications, 2005.(Units I-V)
2. Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & Sons Inc.2002.(Unit-II)

Reference Books:

1. Peter Marwedel, "Embedded System Design", Science Publishers, 2007.
2. Arnold S Burger, "Embedded System Design", CMP.
3. Rajkamal, "Embedded Systems: Architecture, Programming and Design", TMH Publications, Second Edition, 2008.

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Professional Elective - III

ADVANCED COMPTUER NETWORKS

II Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives

To make the students

- understand Congestion & Quality of Service(QoS) techniques in Networks.
- familiarize with the concepts of wireless LAN, WPAN, WWAN and MAN's.
- gain knowledge about cellular systems and ATM Reference model & AAL Layers.

Course Outcomes

Upon successful completion of the course, the students will be able to

- use appropriate congestion control principles Qos Techniques and given network.
- differentiate various wireless networks.
- analyze various cellular systems.
- design ATM networks.
- analyze the various network algorithms.

Course Content

UNIT-I: Congestion and Quality of Service (QoS)

Data traffic, congestion, congestion control, two examples, quality of service, techniques to improve QOS, integrated services and differential services. Queue management: passive-drop trial, drop front, random drop, active- early random drop, random early detection.

UNIT-II: X.25 Standards

X.25 Layers, X.21 protocol ,frame relay: introduction, frame relay operation, frame relay layers, congestion control, leaky bucket algorithms, ATM: Design goals, ATM architecture, switching, switch Fabric, ATM layers, service classes, ATM applications.

UNIT-III: Interconnection Networks

Introduction, Banyan networks, properties, crossbar switch, three stage class networks, rearrangeble networks, folding algorithm, Benes Networks, Lopping

algorithm, bit allocation algorithm. SONET/SDH: synchronous transport signals, physical configuration, SONET layers, SONET frame.

UNIT-IV: Spread Spectrum

Introduction, basic concept, protection against jamming, spreading codes (PN sequence), generation, properties, types of spread spectrum modulation, application of spread spectrum. Private networks: virtual private networks, network address translation next generation: IPV6 Transition from IPV4 to IPV6 ,mobile IP: addressing, agents, three phases, inefficiency in mobile IP

UNIT-V:Wireless Networks

Wireless LAN: IEEE802.11, architecture, MAC sub layer, addressing mechanism, physical layer. Bluetooth: architecture, Bluetooth layers, radio layer, base band layer, L2CAP, wireless WAN: The cellular concept, cell, frequency reuse, principle, channel assignment strategies, interference and system capacity, types of interference, improving capacity in cellular system, handoff, AMPS, D-AMPS, GSM, CDMA, GPRS, 3G & 4G technologies.

Text Books:

1. B. A.Forouzan,"Data Communication and Networking", TMH, 4thedition,2004. (UNITS I-V)
2. B. A. Forouzen, "TCP/IP Protocol Suit ", 4th Edition, TMH.(UNIT IV)

Reference Books:

1. AbhishekYadav, "Wireless Communication System", University Sciences Press.
2. KamiloFeher,"Wireless Digital Communications",PHI,1999.
3. Mahaboob Hassan, Jain Raj, "High Performance TCP-IP Networking", PHI.
4. N. N. Biswas, "ATM Fundamentals" Adventure Book Publishers,1998.

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Professional Elective - III

HARDWARE SOFTWARE CO-DESIGN

II Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives

To make the students

- familiarize with the concepts of hardware/software co-design.
- familiarize with various target architectures and methods of prototyping, emulation, retargetable compilation and verification tools.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- demonstrate the fundamental principles of hardware/software co-design issues.
- understand the methods of prototyping and emulation on target devices.
- understand compilation technologies and languages for system level specification.

Course Content

UNIT – I: Co-Design Issues

Hardware software co-design introduction, issues in co-design - models, architectures, languages; generic co-design methodology.

UNIT – II: Prototyping and Emulation

Introduction, prototyping and emulation techniques, prototyping and emulation environments, architecture specialization techniques, system communication infrastructure.

UNIT – III: Target architectures

Target architectures and application system classes, architecture for control dominated systems (MC68332), data dominated systems (ADSP21060), mixed systems (Intel i960).

UNIT – IV: Compilation Techniques and Embedded Processor Architectures

Modern embedded architectures, embedded software development needs, compilation technologies, practical considerations in a compiler development environment.

UNIT – V: Languages for System Level Specification and Design

System-level specification, design representation for system level synthesis, system level specification languages, heterogeneous specification and multi-language co-simulation.

Text Books:

1. Jorgen Staunstrup, Wayne Wolf, "Hardware/software co- design Principles and Practice", Springer, 2009.

Reference Books:

1. Patrick Schaumont, "A Practical Introduction to Hardware/Software Co-design", 2nd Edition, 2012.
2. R. Gupta, "Co-synthesis of Hardware and Software for Embedded Systems", Kluwer Academic Publishers, 1995.
3. Jean-Michel Bergé, Oz Levia, Jacques Rouillard, "Hardware/Software Co-Design and Co-Verification", Springer, 1997.

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Professional Elective - III

WIRELESS SENSOR NETWORKS

II Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives

To make the students

- familiarize with wireless sensor networks and their architectures.
- understand the MAC, link layer and routing protocols.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- understand the design principles for wireless sensor networks.
- distinguish the functions of different layers.
- apply appropriate routing protocols.
- use various data centric and aggregation techniques for reliable data transfer.

Course Content

UNIT - I: Overview of Wireless Sensor Networks and Architectures

Introduction to sensor networks, comparison of sensor network with Adhoc network, challenges for sensor networks, advantages, applications and enabling technologies for wireless sensor networks. Single-node architecture - hardware components, energy consumption of sensor nodes, operating systems and execution environments, network architecture - sensor network scenarios, design principles for WSNs.

UNIT - II: Physical Layer

Introduction, wireless channel and communication fundamentals – frequency allocation, modulation and demodulation, wave propagation effects and noise, channels models, spread spectrum communication, packet transmission and synchronization, quality of wireless channels and measures for improvement, physical layer and transceiver design considerations in wireless sensor networks-energy usage profile, choice of modulation scheme, dynamic modulation scaling, antenna considerations.

UNIT - III: MAC Protocols and Link Layer Protocols

Fundamentals of wireless MAC protocols, low duty cycle protocols and wakeup concepts, contention based protocols, schedule based protocols, link layer

protocols- fundamental task and requirements, error control, framing, link management.

UNIT - IV: Routing Protocols for Wireless Sensor Networks

Introduction, background, data dissemination and gathering, routing challenges and design issues in wireless sensor networks, routing strategies in wireless sensor networks.

UNIT - V: Data Centric and Content Based Networking and Transport layer

Introduction, data centric routing, data aggregation, data centric storage, the transport layer and QoS in wireless sensor networks, coverage and deployment, reliable data transport single packet delivery, block delivery, congestion control and rate control.

Text Books:

1. Holger Karl and Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks", John Wiley, 2005. (Units: I, II, III, V)
2. Kazem Sohraby, Daniel Minoli and Taieb Znati, " Wireless Sensor Networks Technology, Protocols and Applications", John Wiley & Sons, 2007. (Unit: IV)

Reference Books:

1. Feng Zhao and Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
2. Anna Hac, "Wireless Sensor Network Designs", John Wiley, 2003.
3. C.S.Raghavendra, Krishna M.Sivalingam and TaiebZnati, "Wireless Sensor Networks", Springer Publication, 2004.

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EMBEDDED SYSTEMS LAB

II Semester

Lecture	: 4	Internal Marks	: 40
Credits	: 3	External Marks	: 60

Course Objectives:

To make the students

- familiarize with the Assembly/high level language programming and I/O interfacing of ARM.
- familiarize with verification of concepts in signal processing.

Learning Outcomes

Upon successful completion of the course, the students will be able to

- perform I/O interface with ARM processor.
- perform various signal processing operations using MATLAB.

List of Experiments:

Note: Any four from a to f of part-1and any three from a to d of part-2 to be performed.

Part - 1 :

Assembly/High level language programming and porting it on a ARM processor

a. 32-bit Booth multiplier.
b. 32-bit ALU with addition, subtraction and multiplication operations.
c. Simulate an elevator movement.
d. Read data from a sensor and process.
e. Transmission and reception of serial data.
f. I2C Interface on IDE environment.
g. Design of embedded controller (Open ended).

Part-2

The following experiments are to be implemented on MATLAB environment.

a. DFT calculations.
b. Correlation of given sequences.
c. Power spectral density calculations.
d. Decimation and interpolation.

References:

1. Stephen B Furber , “ARM system on chip Architecture”, Pearson Publications, 2nd edition.
2. G. John Proakis and G. Dimitris Manolakis, “Digital Signal Processing, Pearson Education”, 4th edition.
3. Ze Tian, Dun-shan Yu, and Yu-lin Qiu, “A high effective algorithm of 32-bit multiply and MAC instructions’ VLSI implementation with 32/spl times/8 multiplier-accumulator in DSP applications” 6th IEEE International Conference on Signal Processing, 26-30 Aug. 2002, Beijing, China, China.
4 https://www.pantechsolutions.net/microcontroller-tutorials/how-to-interface-lm35-sensor-with-lpc2148-arm7-starter-board.

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