ACADEMIC REGULATIONS
COURSE STRUCTURE
AND
DETAILED SYLLABUS

VLSI DESIGN & EMBEDDED SYSTEMS

Department of
Electronics and Communication Engineering

M.Tech Two Year Degree Course

(Applicable for the batch admitted from 2020-21)

GUDLAVALLERU ENGINEERING COLLEGE

(An Autonomous Institute with Permanent Affiliation to JNTUK, Kakinada)

Seshadri Rao Knowledge Village

GUDLAVALLERU - 521 356, Krishna District, Andhra Pradesh

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VISION & MISSION OF THE COLLEGE

Vision

To be a leading institution of engineering education and research, preparing students for leadership in their fields in a caring and challenging learning environment.

Mission

- To produce quality engineers by providing state-of-the-art engineering education.
- To attract and retain knowledgeable, creative, motivated and highly skilled individuals whose leadership and contributions uphold the college tenets of education, creativity, research and responsible public service.
- To develop faculty and resources to impart and disseminate knowledge and information to students and also to society that will enhance educational level, which in turn, will contribute to social and economic betterment of society.
- To provide an environment that values and encourages knowledge acquisition and academic freedom, making this a preferred institution for knowledge seekers.
- To provide quality assurance.
- To partner and collaborate with industry, government, and R and D institutes to develop new knowledge and sustainable technologies and serve as an engine for facilitating the nation's economic development.
- To impart personality development skills to students that will help them to succeed and lead.
- To instil in students the attitude, values and vision that will prepare them to lead lives of personal integrity and civic responsibility.
- To promote a campus environment that welcomes and makes students of all races, cultures and civilizations feel at home.
- Putting students face to face with industrial, governmental and societal challenges.

VISION & MISSION OF THE DEPARTMENT

Vision

To be a leading centre of education and research in Electronics and Communication Engineering, making the students adaptable to changing technological and societal needs in a holistic learning environment.

Articulations

- To be a leading centre of education and research hub in Electronics and Communication Engineering with holistic learning environment.
- Students to be adaptable for the changes in technology and societal needs.
- Students to be recognized and valued for their commitment to excellence and enthusiasm for learning.

Mission:

- To produce knowledgeable and technologically competent engineers for providing services to the society.
- To have a collaboration with leading academic, industrial and research organizations for promoting research activities among faculty and students.
- To create an integrated learning environment for sustained growth in electronics and communication engineering and related areas.

Articulations

- To craft the graduates knowledge and technologically competent engineers for providing services to the society.
- To have alliance with leading academicians, industries and research organizations and encourage the faculty and students for performing research activities.
- To develop a multidiscipline learning environment for continuous growth in electronics and communication engineering and its associated fields.

III. PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

To make the graduates of M.Tech Programme in VLSI Design and Embedded Systems

PEO-I : Identify and use appropriate modern tools to solve real world problems in VLSI Design and Embedded Systems domain.

PEO-II : Develop an ability of writing and presenting a substantial technical report/ document and demonstrate degree of mastery over the area of specialization.

PEO-III: Inculcate self learning to pursue research career in relevant areas.

IV. PROGRAM OUTCOMES (POs)

The Post-Graduates will be equipped with an ability to

PO-1 : independently carry out research /investigation and development work to solve practical problems.

PO-2 : write and present a substantial technical report/document.

PO-3 : demonstrate a degree of mastery over the area as per the specialization of the program.

V. ACADEMIC REGULATIONS

Applicable for the students of M.Tech from the Academic Year 2020-21.

1. PG – M.Tech Programs

The following M.Tech Programs are offered at present

i. Structural Engineering (SE)
ii. Power Electronics and Electric Drives (PEED)
iii. Machine Design (MD)
iv. VLSI Design and Embedded Systems (VLSID & ES)
v. Computer Science and Engineering (CSE)

2. Duration of the Program

The duration of the program is two academic years consisting of four semesters. However, a student is permitted to complete the course work of M.Tech program in the stipulated time frame of four academic years from the date of joining.

3. Minimum Instruction Days

Each semester consists of a minimum of ninety instruction days.

4. Program Credits

Each specialization of the M.Tech programs is designed to have a total of 70 credits and the student shall have to complete the two year course work and earn all the 70 credits for the award of M.Tech Degree.

5. Attendance Regulations

5.1 A student shall be eligible to appear for Semester End Examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.

5.2 Condoning of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester will be considered for genuine reasons such as medical grounds and participation in co-curricular and extra-curricular activities and shall be granted only after approval by the College Academic Committee. Student should submit application for medical leave along with medical certificate from a registered medical practitioner within three days from reporting to the class work after the expiry of the medical leave. In case of participation in co-curricular and extra-curricular activities, either in the college or other colleges, students must take prior written permission from HoD concerned and should also submit the certificate of participation from the organizer of the event within three days after the completion of the event. Only such cases will be considered for condoning attendance shortage.

5.3 A student shall be eligible to claim for condonation of attendance shortage only once during the two years (four semesters) course work.

5.4 A student will not be promoted to the next semester unless he satisfies the attendance requirement of the current semester. He may seek re-admission for that semester when offered next.

5.5 Shortage of Attendance below 65% in aggregate shall in *NO* case be condoned.

5.6 Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examination of that semester and their registration shall stand cancelled.

5.7 A fee stipulated by the college shall be payable towards condoning attendance shortage.

5.8 A Student is required to put up a minimum of 75% attendance in the Mandatory Non-credit courses for getting the satisfactory grade.

6. Examinations and Scheme of Evaluation

6.1 Theory Courses :

Each theory course shall be evaluated for a total of 100 marks, consisting of 30 marks for internal assessment and 70 marks for semester end examination.

Internal Assessment:

i) Of 30 marks for internal assessment, 10 marks are for continuous assessment in the form of two assignments and 20 marks are based on two mid-term examinations.

ii) Each assignment carries 10 marks and the average of two assignments shall be taken as the marks for continuous assessment.

iii) Each mid-term examination is conducted for 30 marks with one and half hour duration. Each mid-term examination consists of three questions, each for 10 marks. All the questions need to be answered.

iv) Sum of the75% marks of better scored mid-term examination and 25% marks of less scored mid-term examination are scaled down for 20 marks.

v) For the project based theory course, the distribution of 30 marks for internal evaluation shall be 20 marks for theory, based on two mid- term examinations and 10 marks for project. Each mid-term examination is conducted for 30 marks with one and half hour duration. Each mid-term examination consists of two questions, each for 15 marks, with internal choice. All the questions need to be answered. Sum of the 75% marks of better scored mid-term examination and 25% marks of less scored mid-term examination are scaled down for 20 marks.

External Assessment:

i) Semester End Examination will be conducted for 70 marks consisting of five internal choice questions i.e. "either" or choice, carrying 14 marks each. There will be two questions from each unit and the student should answer either of the two questions.

ii) For the project based theory course, the pattern of semester end examination is same as the above. There will be no external assessment for project component.

6.2 Laboratory Courses :

i) For practical subjects the distribution shall be 30 marks for Internal Evaluation and 70 marks for the End Examination. There shall be continuous evaluation by the internal subject teacher during the semester for 30 internal marks. Of the 30 marks for internal, 20 marks shall be for day-to-day performance (15 marks for day-to-day evaluation and 5 marks for Record) and 10 marks shall be evaluated by conducting an internal laboratory test towards the end of semester.

ii) Semester end examination shall be conducted by an internal examiner and an external examiner for 70 marks.

6.3 Mini Project with Seminar:

Mini Project with seminar shall be evaluated for a total of 100 Marks.

i) Of 100 marks, 30 marks shall be awarded by the project supervisor based on student's involvement in carrying out the project and the remaining 70 marks are based on presentation and viva-voce before a committee consisting of supervisor, head of the department and a senior faculty of the department.

ii) There will be no external assessment for mini project.

6.4 Mandatory Non-credit Course:

i) A student is required to take up two Non-Credit course viz. Constitution of India, English for Research Paper writing, one in I semester and the other in II semester. Marks are awarded based on the day-to-day performance in the seminars organized under each course. A student is required to score 40 marks out of 100 marks despite putting up a minimum of 75% attendance to be declared satisfactory in each mandatory non-credit course. The M.Tech degree shall only be awarded if a student gets satisfactory grade in each of the two mandatory non-credit courses and besides acquiring 70 credits of the M.Tech degree course.

ii) A student whose shortage of attendance is condoned in the case of credit courses in that semester shall also be eligible for condoning shortage of attendance up to 10% in the case of mandatory non-credit courses also.

iii) A student has to repeat the course whenever it is offered, if he does not get satisfactory grade or not fulfilling the attendance requirements in each non-credit course for getting the degree awarded.

6.5 MOOCs:

i) A Student shall register for MOOCs offered by NPTEL, CISCO, MICROSOFT and SAYLOR or any other agency with prior approval of departmental committee.

ii) The courses should be other than those offered under regular curriculum and are to be approved by the Departmental Committee consisting of the head of the department, mentor and one/two senior faculty members before the commencement of each semester.

iii) The duration of the course shall be 12 weeks / 50-70 hrs (maximum).

iv) The schedule of the course must be in line with the academic schedule of that semester.

v) The required credits shall be awarded on submission of certificate from the approved agency.

6.6 Project Work:

Every candidate shall be required to submit a dissertation on a topic approved by the Project Review Committee.

i) A Project Review Committee (PRC) shall be constituted for each specialization with Head of the Department / a Senior Faculty as Chairman and two other senior faculty members.

ii) Registration of Project Work: A candidate who has been promoted to 3rd semester shall be eligible to register for the project work.

iii) The eligible candidate can choose his project supervisor and submit the title, objective, abstract and plan of action of the proposed project work to the department for approval by the PRC. The candidate whose proposal is approved by the PRC shall register for the project work. The minimum duration of project work will be 36 weeks from the date of registration.

iv) If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. In case of such changes, the candidate has to register afresh.

v) There shall be three reviews on the progress of the project work by the PRC with an interval of 12 weeks. The candidate needs to submit a report on the progress of his work and present it before the PRC for assessment. The PRC may suggest for an extension of date of submission of dissertation if the progress of work is not satisfactory or absent himself for the review.

vi) A candidate who has passed all the theory, laboratory and Mini project with seminar examinations and shown satisfactory progress of project work is permitted to submit the dissertation after 36 weeks from the date of registration.

vii) If a candidate fails to submit the dissertation by the end of the 4th semester, he has to take the permission for an extension by paying the semester(s) tuition fee.

viii) Three copies of the Project Thesis certified by the supervisor shall be submitted to the Department.

ix) Project evaluation and Viva-Voce examination is conducted at the end of 4th semester by a committee consisting of Project Supervisor, senior faculty of the department, HoD and an External Examiner nominated by the Chief Controller of Examinations out of a panel of three examiners suggested by the department.

The following grades are awarded for the project work:

i. Excellent
ii. Very Good
iii. Good
iv. Satisfactory
v. Unsatisfactory

The Grade "unsatisfactory" is treated as Fail. Failed Students should take supplementary examination after making required modifications, if any, in the dissertation with a minimum gap of 8 weeks by paying the required examination fee.

7. Criteria for Passing a Course and Award of Grades:

7.1 Criteria for Passing a Course:

i) A candidate shall be declared to have passed in individual theory / laboratory course, if he secures a minimum of 50% aggregate marks (internal & semester end examination marks put together), subject to securing a minimum of 40% marks in the semester end examination.

ii) The candidate shall be declared to have passed in Mini project with seminar if he secures 50% marks.

iii) The candidate shall be declared to have successfully completed the project work if he secures a minimum of 'satisfactory' grade in the project evaluation and viva-voce examination.

iv) On passing a course of a program, the student shall earn assigned credits in that course.

7.2 Method of Awarding Letter Grade and Grade Points for a Course:

A letter grade and grade points will be awarded to a student in each course based on his performance, as per the grading system given below.

Theory /Elective /Laboratory /Seminar / Term Paper /Project Dissertation (%)	Grade Points	Letter Grade
≥ 90	10	O (Outstanding
≥ 80 & < 90	9	A+ (Excellent)
≥ 70 & < 80	8	A (Very Good)
≥ 60 & < 70	7	B+ (Good)
≥ 50 & < 60	6	B (Above Average)
< 50	0	F (Fail)

7.3 Calculation of Semester Grade Point Average (SGPA)* for semester:

The performance of each student at the end of the each semester is indicated in terms of SGPA. The SGPA is calculated as given below:

SGPA = $\frac{\sum(CR \, X \, GP)}{\sum CR}$ for each semester.

where CR = Credits of a course

GP = Grade Points awarded for a course

* SGPA is calculated for a candidate who passed all the courses in that semester.

7.4 Eligibility for Award of M.Tech Degree:

A student will be declared eligible for the award of the M. Tech. Degree if he fulfills the following academic regulations.

(a) Pursued a course of study for not less than two academic years and not more than four academic years.

(b) Registered for prescribed **70** credits and secured **70** credits.

(c) Students, who fail to complete their Two years Course of study within Four years or fail to acquire the prescribed **70** Credits for the award of the degree within four academic years from the year of their admission shall forfeit their seat in M. Tech course and their admission shall stand cancelled.

7.5 Calculation of Cumulative Grade Point Average (CGPA) for Entire Program:

The CGPA is calculated as given below:

CGPA = $\frac{\sum(CR \, X \, GP)}{\sum CR}$ for entire program.

where CR = Credits of a course

GP = Grade points awarded for a course

* CGPA is calculated for a candidate who passed all the prescribed courses excluding project work.

7.6 Award of Division:

After satisfying the requirements prescribed for the completion of the program, the student shall be eligible for the award of B.Tech Degree and shall be placed in one of the following grades:

CGPA	Class
≥ 7.5	First Class with Distinction *
≥ 6.5 & < 7.5	First Class
≥ 6.0 & < 6.5	Second Class

*** CGPA** ≥ 7.5 will be awarded first class with distinction provided the student must have fulfilled all the program requirements in two (2) years duration.

8. Supplementary Examinations

i) Supplementary examinations will be conducted once in a year along with regular examinations.

ii) Semester end supplementary examinations shall be conducted till next regulation comes into force for that semester after the conduct of the last set of regular examinations under the present regulation.

iii) Thereafter supplementary examinations will be conducted in the equivalent courses as decided by the Board of Studies concerned.

9. Challenge Valuation

Challenge valuation of failed or passed subjects shall be performed as per the following norms.

i) Students can submit the application for challenge valuation, along with the prescribed fee receipt for evaluation of his answer script(s) of theory course(s) as per the notification issued by the Controller of Examinations.

The Controller of Examinations shall arrange for challenge valuation of such answer script(s).

ii) The challenge valuation will be carried out by a three member committee comprising an external subject expert nominated by the Chief Controller of Examinations, the internal subject expert and the BoS Chairman.

iii) After the challenge valuation, if the grade is improved or there is a change in the status i.e., fail to pass, the improved grade shall be notified, otherwise, the previous grade will remain.

10. Re-admission Criteria

A candidate, who is detained in a semester due to lack of attendance has to obtain written permission from the Principal for readmission into the same semester after duly fulfilling the required norms stipulated by the college and by paying the required tuition fee and special fee in addition to paying an administrative fee of Rs. 1,000/-

11. Break in Study

Student, who discontinues the studies for what-so-ever reason, can get readmission into appropriate semester of M.Tech program only with the prior permission of the Principal of the College, provided such candidate shall follow the transitory regulations applicable to the batch he joins. An administrative fee of Rs.2,000/- per each year of break in study in addition to the prescribed tuition and special fees shall be paid by the candidate to condone his break in study.

12. Transitory Regulations

When a student is detained due to shortage of attendance, he/she may be readmitted into the same semester in which he/she has been detained. However, the academic regulations under which the detained student was first admitted shall continue to be applicable to him/her. A candidate, who is detained in a semester, on readmission shall be required to do all the courses in the curriculum prescribed for the batch of students in which the student joins subsequently. However, exemption will be given to those candidates who have already passed such courses in the earlier semester(s) he was originally admitted into and he will be offered substitute subjects in place of them as decided by the Board of Studies. However, the decision of the Board of Studies will be final.

13. Withholding of Results

If the student has not paid the dues, if any, to the College or if any case of indiscipline is pending against him, the result of the student will be withheld. His degree will be withheld in such cases.

14. Malpractices

i) The Principal shall refer the cases of malpractices in internal assessment tests and semester end examinations to a malpractice enquiry committee constituted by him for the purpose. Such committee shall follow the approved levels of punishment. The Principal shall take necessary action against the erring students based on the recommendations of the committee.

ii) Any action by the candidate trying to get undue advantage in the performance or trying to help another, or derive the same through unfair means is punishable according to the provisions contained hereunder.

iii) Malpractices identified at spot centre during valuation

The following procedure is to be followed in the case of malpractice cases detected during valuation, scrutiny etc. at spot centre.

I. A notice is to be served to the candidate(s) involved **(i)** through the Principal of the college, **(ii)** to the candidate(s) to his college address and **(iii)** to the candidate(s) to his permanent address regarding the malpractice.

DISCIPLINARY ACTION FOR MALPRACTICES/IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices / Improper conduct	Punishment
If the candidate		
1.a	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination.)	Expulsion from the examination hall and cancellation of the performance in that subject only.
b	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through Cell phones with any candidates or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester / year. The hall ticket of the candidate shall be cancelled.

3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for the examinations of the remaining subjects of that semester / year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the impostor is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or takes out or arranges to send out the question paper during the examination or answer book during or after the examination.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester / year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of performance in that subject.

6.	Refuses to obey the orders of the Chief Superintendent/Assistant Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in or around the examination hall or organises a walkout or instigates others to walkout or threatens the officer-in-charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the Officer-in-charge or any person on duty in or outside the examination hall of any of his relations or indulges in any other act of misconduct or mischief which results in damage to or destruction of property in the examination hall or any part of the college campus or engages in any other act which in the opinion of the Officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	Expulsion from the examination hall and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester / year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The candidate is also debarred for two consecutive semesters from class work and all university examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The candidate is also debarred and forfeits the seat.

9	If student of the college who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the college will be handed over to the police and a police case is registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester / year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester / year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be referred to the Chief Superintendent of Examinations for future action towards suitable punishment.	

II. A committee consisting of the following is to be constituted at spot centre to process such malpractice cases and the recommendations of the malpractice committee are to be sent to the Chief Controller of Examinations.

1. Principal — Chairman
2. Vice Principal - Academics — Member
3. Chief examiner of that subject — Member
4. Controller of Examinations — Convener

The involvement of the staff, who are in charge of conducting examinations, valuing examination papers and preparing / keeping records

of documents related to the examinations in such acts (inclusive of providing incorrect or misleading information) that infringe upon the course of natural justice to one and all concerned at the examination shall be viewed seriously and appropriate disciplinary action will be taken after thorough enquiry.

15. Other Matters

i) Deserving physically challenged candidates will be given additional examination time and a scribe based on the certificate issued by the concerned authority. Students who are suffering from contagious diseases are not allowed to appear either for internal or semester end examinations.

ii) The students who participated in coaching / tournaments held at State / National / International levels through University / Indian Olympic Association during semester end external examination period will be promoted to subsequent semesters as per the guidelines of University Grants Commission Letter No. F.1-5/88 (SPE/PES), dated 18-08-1994.

iii) The Principal shall deal in an appropriate manner with any academic problem which is not covered under these rules and regulations, in consultation with the Heads of the Departments and subsequently such actions shall be placed before the Academic Council for ratification. Any emergency modification of regulation, approved in the meetings of the Heads of the Departments shall be reported to the Academic Council for ratification.

16. General

i) The Academic Council may, from time to time, revise, amend or change the regulations, schemes of examination and /or syllabi.

ii) The academic regulations should be read as a whole for the purpose of any interpretation.

iii) In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman of the Academic Council is final.

v) Wherever the word he, him or his occurs, it will also include she, her and hers.

VI. CURRICULAR COMPONENT

Sl. No.	Course Work - Subject Areas	Total No.of Credits	% of Total Credits
1	Open Elective (OE)	3	4.29
2	Humanities and Social Sciences (HSS)	3	4.29
3	Professional Core (PC)	20	28.58
4	Professional Electives (PE)	15	21.42
7	Others (Seminar, Term Paper, Dissertation, etc.)	29	41.42

COURSE STRUCTURE

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SYLLABUS

COURSE STRUCTURE

I Semester

Sl. No.	Course Code	Name of the Course / Laboratory	No.of Periods per week			No.of Credits
			L	T	P	
1	EC4901	CMOS VLSI Design	3	-	-	3
2	EC4902	Advanced Microcontrollers *	3	-	-	3
3		Professional Elective - I	3	-	-	3
4		Professional Elective - II	3	-	-	3
5	BA3901	Research Methodology & IPR	3	-	-	3
6	EC4909	CMOS VLSI Design Lab	-	-	4	2
7	EC4910	Advanced Microcontrollers Lab	-	-	4	2
		Total	**15**	**-**	**8**	**19**
8	BA3902	Constitution of India (Audit Course)	2	-	-	

II Semester

Sl. No.	Course Code	Name of the Course / Laboratory	No.of Periods per week			No.of Credits
			L	T	P	
1	EC4911	VLSI System Design *	3	-	-	3
2	EC4912	Embedded System Based IoT	3	-	-	3
3		Professional Elective - III	3	-	-	3
4		Professional Elective - IV	3	-	-	3
5	EC4919	VLSI System Design Lab	-	-	4	2
6	EC4920	Embedded System and IoT Lab	-	-	4	2
7	EC4921	Mini Project with Seminar	-	-	6	3
		Total	**12**	**-**	**14**	**19**
8	EG3901	English for Research Paper Writing (Audit Course)	2	-	-	-

III Semester

Sl. No.	Course Code	Name of the Course / Laboratory	No.of Periods per week			No.of Credits
			L	T	P	
1		Professional Elective - V	3	-	-	3
2		Open Elective	3	-	-	3
3	EC4925	Dissertation Phase - I	-	-	20	10
		Total	**6**	**-**	**20**	**16**

* Project Based Theory Course

L : Lecture **T : Tutorial** **P : Practical**

IV Semester

Sl. No.	Course Code	Name of the Course / Laboratory	No.of Periods per week			No.of Credits
			L	T	P	
1	EC4925	Dissertation Phase - II	-	-	32	16
		Total	**-**	**-**	**32**	**16**

Professional Electives:

Professional Elective - I

EC4903 Testing and Testability of VLSI Circuits
EC4904 Advanced Digital Design
EC4905 Digital Signal and Image Processing

Professional Elective - II

EC4906 VLSI Signal Proessing
EC4907 System Design with Embedded Linux
EC4908 Parallel Processing

Professional Elective - III

EC4913 Advances in VLSI Design
EC4914 Embedded Computer Architecture
EC4915 System on Chip Design

Professional Elective - IV

EC4916 VLSI Interconnects
EC4917 Communication Buses and Interfaces
EC4918 Advanced Digital Signal Processing

Professional Elective - V

EC4922 Lower Power VLSI Design
EC4923 Network Security and Crypthography
EC4925 MOOCs

Open Electives:

CE3924 Sustainable Development
EE3924 Energy Audit, Conservation & Management
ME3924 Rapid Prototyping
EC4924 Automotive Electronics (Otther than VLSID&ES)
CS3924 Soft Computing Techniques

SYLLABUS

CMOS VLSI DESIGN

I Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To acquaint with the MOSFET behaviour and models.
- To understand the behaviour of CMOS inverter and concepts of designing combinational and sequential circuits.
- To familiarize with the operation of MOSFET amplifiers, operational amplifiers and switched-capacitor circuits.

Course Outcomes

Upon successful completion of the course, the students will be able to

- understand the behaviour of CMOS inverter and its energy dissipation.
- design CMOS inverter and calculate delay times using mathematics and basic engineering concepts.
- analyze combinational and sequential logic circuits; single-stage, cascode, and differential amplifiers; current mirrors, and switched-capacitor circuits.
- understand the operation of one-stage and two-stage op amps.

Course Content

UNIT– I: The CMOS Inverter

Static CMOS inverter, static behaviour, dynamic behaviour, power, energy, and energy-delay.

UNIT–II: Designing Combinational Logic Gates in CMOS

Static CMOS design, dynamic CMOS design, designing logic for reduced supply voltages.

UNIT–III: Designing Sequential Logic Circuits

Introduction, static latches and registers, dynamic latches and registers, alternative register styles, pipelining, Non-bistable sequential circuits.

UNIT–IV: MOS Device Models and Amplifiers

Second-order effects in MOS devices, MOS device models, common-source stage, source follower, common-gate stage, cascode stage, single-ended and differential operation, basic differential pair, basic and cascode current mirrors.

UNIT–V: Operational Amplifiers and Switched-Capacitor Circuits

General considerations for op amps, one-stage op amps, two-stage op amps, general considerations for switched-capacitor circuits, sampling-switches,

switched-capacitor amplifiers, switched-capacitor integrator, switched-capacitor common-mode feedback..

Text Books

1. Jan M. Rabaey, “Digital Integrated Circuits-A Design Perspective”, Prentice Hall Inc., 2nd Edition (Units: I – III)
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw-Hill Education, Second Edition, 2017. (Units: IV & V).

Reference Books

1. Neil Weste and David Harris, “CMOS VLSI Design: A Circuits and Systems Perspective, Pearson Education, 4th Edition.
2. Sung-Mo Kang and Yusuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, McGraw-Hill, 3rd Edition.
3. Paul R. Gray, Paul J. Hurst, Stephen H. Lewls, Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits”, John Wiley & Sons, 4th Edition, 2001.
4. Tony Chan Carusone, David A. Johns, Kenneth W. Martin, “Analog Integrated Circuit Design”, John Wiley & Sons, 2nd Edition, 2012.

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ADVANCED MICROCONTROLLERS

I Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with architecture and the instruction set of different microcontrollers.
- To familiarize with assembly language programming of various microcontrollers.

Course Outcomes

Upon successful completion of the course, the students will be able to

- understand the internal architecture of Atmel, PIC and ARM microcontrollers.
- identify the suitable ARM core to develop embedded applications.
- discriminate the performance of different microcontrollers.

Course Content

UNIT – I: Atmel Microcontrollers

Introduction to Atmel microcontrollers (89CXX and 89C20XX), architectural overview and pin description of 89C51 and 89C2051, precision analog comparator in 89C2051, ADC using precision analog comparator, power saving options, pulse generation, PWM, pulse width measurement and frequency counter.

UNIT – II: PIC Microcontrollers

Overview and features, PIC 16C6X/7X: architecture, addressing modes, instruction set, memory organization, I/O ports, interrupts, timers, ADC. PIC 16F8XX: pin diagram, program memory, data memory, Interrupts, I/O ports and timers. CCP module in PIC 16F877, MSSP module, USART.

UNIT – III: ARM Cortex-M3 Processor

Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

UNIT – IV: Interrupts

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration.

UNIT – V: LPC17xx Microcontroller

Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

Text Books

1. Ajay V Deshmukh, "Microcontrollers-Theory and Applications", TMH Publications, 1st Edition, 2005 (Units-I-II).
2. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition. (Units III-V).
3. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication.

Reference Books

1. M. Ali Mazidi and J. Gillispie Mazidi , "The 8051 Microcontroller and Embedded Systems using Assembly and C", 2nd Edition.
2. Lucio Bi Jasio, "PIC Microcontrollers", Newnes Publishers, 1st Edition, 2008.
3. Technical references and user manuals on www.arm.com.

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Professional Elective - I

TESTING AND TESTABILITY OF VLSI CIRCUITS

I Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with the basics of testing techniques.

Course Outcomes

Upon successful completion of the course, the students will be able to

- interpret the concepts of modeling digital circuits
- apply the concepts in testing and verification of a digital design
- identify the design for testability methods for combinational & sequential circuits.
- recognize the BIST techniques for improving testability.

Course Content

UNIT – I: Introduction to Fault Modeling

Modeling Digital circuits at logic level, register level and structural level, levels of modeling, Difference between testing, fault diagnosis and verification. Physical faults and their modeling: stuck-at faults, bridging faults, CMOS stuck-open and stuck-on faults. Fault collapsing: fault equivalence and fault dominance.

UNIT – II: Logic and Fault Simulation

Logic simulation techniques: compiled code, event-driven simulation. Fault simulation techniques: parallel, deductive and concurrent fault simulation, critical path testing. Fault models, fault detection and redundancy, fault equivalence and fault location, fault dominance, automatic test pattern generation.

UNIT – III: Test automation and Design verification

Deterministic test generation for combinational circuits: Exhaustive and pseudo-exhaustive test pattern generation, Pseudo-random test pattern generation, Linear feedback shift register (LFSR), characteristic polynomial, Weighted random pattern generation, Test generation for sequential circuits: time frame expansion method**,** domain.

UNIT – IV: Design for Testability (DFT)

Test pattern generation for sequential circuits: Scan architectures and testing-controllability and observability, generic boundary scan, fully integrated scan, adhoc and structured techniques. Scan path and level sensitive scan design (LSSD). Boundary scan (JTAG) standard.

UNIT – V: Built-in Self-test (BIST)

BIST concepts and test pattern, BIST for testing of logic and memories, Test automation, Specific BIST architectures: BILBO, STUMPS, CSBL, BEST, RTs, LOCST. Introduction to advanced BIST concepts, design for self test at board level.

Text Books

1. M. Abramovici, M. A. Breuer and A. D. Friedman, "Digital Systems Testing and Testable Design", Jaico Publishing House, 1990**.** (Units I-V)

Reference Books

1. N. N. Biswas, "Logic Design Theory", PHI, 2001.
2. Z. Kohavi, "Switching and Finite Automata Theory", TMH, 2nd Edition, 2001.

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Professional Elective - I

ADVANCED DIGITAL DESIGN

I Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with the Synthesis of Combinational and Sequential logic circuits.
- To introduce the techniques and tools for programmable logic design.
- To acquaint with the knowledge of fault diagnosis in combinational and sequential circuits.

Course Outcomes

Upon successful completion of the course, the students will be able to

- synthesize Combinational and Sequential logic circuits
- design and Synthesize the Datapath Controllers..
- program the PLDs..
- model the architectures for Arithmetic Proceesors
- design the state machines using SM charts.

Course Content

UNIT – I: Synthesis of Combinational and Sequential logic

Review of Combinational and Sequential logic design ,Introduction to synthesis ,Synthesis of combinational logic, Synthesis of sequential logic with latches, Synthesis of three state devices and bus interfaces, Synthesis of sequential logic with flipflops, Registered logic, State encoding, Synthesis of gated clocks and clock enables, Anticipating the results of synthesis.

UNIT – II: Design and Synthesis of Datapath Controllers

Partitioned sequential machines, Design example: Binary counter , Design and synthesis of a RISC stored-program machine ,Processor, ALU, Controller, Instruction Set, Controller Design and Program Execution.

UNIT – III: Programmable Logic Devices

Programmability of PLDs, Complex PLDs, Xilinx Virtex FPGA's, Verilog based Design flows for FPGA's, Synthesis with FPGA's, Xilinx Kintex 7 FPGA features, ZynQ SoC features.

UNIT – IV: Architectures for Arithmetic Processors

Review of functional units for addition and subtraction, Functional units for multiplication - combinational binary multiplier, sequential binary multiplier, sequential Multiplier design: Hierarchical decomposition, efficient STG based Sequential bi-

nary Multiplier, Booth's-Algorithm Sequential Multiplier, Multiplication of signed Binary numbers, Multiplication of fractions.

UNIT – V: State Machine Design with SM charts

State Machine charts, Derivation of SM charts, Realization of SM charts, Fundamental state Model-Flow Table-State Reduction-Minimal Close d covers, Races, cycles, Hazards.

Text Books

1. Michael D. Ciletti, "Advanced Digital Design with the VERILOG HDL, 2nd Edition, Pearson Education, 2010. (Units: I, II, III, IV).
2. Charles H.Roth, "Fundamentals of Logic Design", TMH, 7th Edition. (Unit: V)

Reference Books

1. Stephenbrown, "Fundamentals of Digital Logic with Verilog", McGraw-Hill-2007
2. Samuel C. Lee, "Digital Circuits and Logic Design", PHI, 1st Edition.
3. https://www.xilinx.com/products/silicon-devices/fpga/kintex-7.html (Unit: III)
4. https://www.xilinx.com/support/documentation/data_sheets/ds190-Zynq-7000-Overview.pdf (Unit: III)

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Professional Elective - I

DIGITAL SIGNAL AND IMAGE PROCESSING

I Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To introduce the concepts of Z-transform and frequency domain representation of discrete time signals and to familiarize with the designing of digital filters and finite word length effects.
- To introduce fundamental concepts of image processing and different operations on image elements. and expose to the practical problems associated with processing of an image.

Course Outcomes

Upon successful completion of the course, the students will be able to

- select appropriate type of sensors and actuators for a robot manipulator.
- analyze discrete-time signals and systems in various domains (i.e Time, Z and Fourier)
- design the digital filters (both IIR and FIR) from the given specifications
- analyze the quantization effects in digital filters and understand the basics of image sampling, quantization and image transforms.
- understand the concepts of image enhancement, image restoration and image segmentation.
- know the various methods involved in image compression and fundamentals in color image processing.

Course Content

UNIT – I:

Review of Discrete Time signals and systems, Characterization in time, Z and Fourier domain, Fast Fourier Transform using Decimation In Time (DIT) and Decimation In Frequency (DIF) Algorithms.

UNIT – II:

IIR Digital Filters: Introduction, Analog filter approximations – Butter worth and Chebyshev, Design of IIR Digital filters from analog filters using Impulse Invariance, Bilinear Transformation methods.

FIR Digital Filters: Introduction, Design of FIR Digital Filters using Window Techniques, Frequency Sampling technique, Comparison of IIR & FIR filters

UNIT – III:

Analysis of Finite Word length Effects: The Quantization Process and Errors, Quantization of FixedPoint Numbers, Quantization of Floating-Point Numbers, Analysis of Coefficient Quantization effects.

Introduction to Digital Image Processing: Introduction, components in image processing system, Applications of Digital image processing, Image sensing and acquisition, Image sampling, Quantization, Basic Relationships between pixels, Image Transforms: 2D-DFT, DCT, Haar Transform.

UNIT – IV:

Image Enhancement: Intensity transformation functions, histogram processing, fundamentals of spatial filtering, smoothing spatial filters, sharpening spatial filters, the basics of filtering in the frequency domain, image smoothing using frequency domain filters, Image Sharpening using frequency domain filters, Selective filtering.

Image Restoration: Introduction, restoration in the presence of noise only-Spatial Filtering, Periodic Noise Reduction by frequency domain filtering, Linear, Position –Invariant Degradations, Estimating the degradation function, Inverse filtering, Minimum mean square error (Wiener) filtering.

Image Segmentation: Fundamentals, point, line, edge detection, thresholding, region based segmentation.

UNIT – V:

Image Compression: Fundamentals, Basic compression methods: Huffman coding, Arithmetic coding, Run-Length coding, Block Transform coding, Predictive coding, Wavelet coding.

Color Image Processing: color fundamentals, color models, pseudo color image processing, basics of full color image processing, color transformations, smoothing and sharpening. Image segmentation based on color, noise in color images, color image compression.

Text Books

1. John G. Proakis, Dimitris G.Manolakis, “Digital Signal Processing, Principles, Algorithms, and Applications”, PearsonEducation/PHI,2007.
2. S. K. Mitra. “Digital Signal Processing – A Computer based Approach”, TMH, 3rd Edition, 2006
3. Rafael C.Gonzalez and Richard E. Woods, “Digital Image Processing”, Pearson Education, 2011.
4. S.Jayaraman, S.Esakkirajan, T.Veerakumar, “Digital Image Processing”, Mc Graw Hill Publishers, 2009.

Reference Books

1. Digital Signal Processing: Andreas Antoniou, TATA McGraw Hill , 2006 2. Digital Signal Processing: MH Hayes, Schaum s Outlines, TATA Mc-Graw Hill, 2007.
2. Anil K. Jain, “Fundamentals of Digital Image Processing,” Prentice Hall of India, 2012.

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Professional Elective - II

VLSI SIGNAL PROCESSING

I Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with the basic concepts of DSP algorithms.
- To Introduce the various pipelining and parallel processing techniques.

Course Outcomes

Upon successful completion of the course, the students will be able to

- apply DSP algorithms on to the IC technology
- realize the concept of Retiming, unfolding in VLSI based DSP
- analyze the concept of pipelining and processing for DSP
- optimize the Delay using Folding.

Course Content

UNIT – I:

Introduction: A Digital Signal- Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation, Q-Notation.

UNIT – II:

Basic FIR filter, architectures, Simple Block diagrams and Signal flow graphs, Dataflow Graphs, Iteration Period, FIR filter iteration period, IIR filter iteration period, Computation Model, Constraint analysis for IPB computation, Motivational examples for IPB, General IPB computation.

UNIT – III:

Parallel architecture, Odd-even register reuse, Power consumption, Pipelining, Pipelining FIR filter, Time-invariant systems, Valid pipelining examples, Balanced pipeline, Retiming theorem and concept, Retiming IIR filter, ASAP schedule, Utilization Efficiency, Iteration period bound and scheduling.

UNIT – IV:

Pipelining and parallel processing, pipelining of FIR Digital Filters, Pipelining and parallel processing for low power. Systolic architecture design: systolic array design Methodology.

UNIT – V:

Folding of DFG, Folding Examples - IIR Filter, Retiming for folding, Introduction to Delay Optimization by Folding, Parallel implementation of FIR filters, Unfolding Transformation, Look ahead Transformation.

Text Books

1. Keshab K.Parhi Design and Implementation", "VLSI Digital Signal Processing systems", Wiley, Inter Science, 1999. (ISBN Number: 0-471-24186-5).
2. Avatar Singh and S. Srinivasan, "Digital Signal Processing", Thomson Learning, 2004.

Reference Books

1. S.Y. Kung, H.J. White House, T.Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.
2. John G.Proakis, Dimitris G.Manolakis "Digital Signal Processing", Prentice Hall of India, 1995.

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Professional Elective - II

SYSTEM DESIGN WITH EMBEDDED LINUX

I Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with embedded Linux development model.
- To develop various embedded drivers such as the Serial driverand USB gadgets.

Course Outcomes

Upon successful completion of the course, the students will be able to

- familiarize with embedded Linux development model.
- developsimpleembedded Linux drivers.
- develop basic Board Support Packages.
- familiarize with porting, building and debugging applications.

Course Content

UNIT–I: Introduction to Embedded Linux

Embedded Linux , Vendor Independence, Time to Market,Varied Hardware Support, Open Source,Standards (POSIX®) Compliance, Embedded Linux Versus Desktop Linux, Embedded LinuxDistributions, BlueCat Linux, Cadenux , Denx, Embedded Debian (Emdebian),ELinOS (SYSGO),Metrowerks ,MontaVista Linux, RTLinuxPro, TimeSys Linux, Basic commands.

UNIT–II: Overview

Embedded Linux Architecture, Real-Time Executive, Monolithic Kernels, Microkernel-Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC,User space, Start-up sequence, Boot Loader Phase, Kernel Start-Up, User Space Initialization.

UNIT–III: Board Support Package and Embedded Storage

Board Support Package definition, Embedded Storage: Flash Map, MTD Architecture-NAND vs NOR, Embedded File Systems,Optimizing Storage Space,Tuning Kernel Memory.

UNIT–IV: Embedded Drivers

Overview: Serial,USB, watchdog Timer, Kernel Modules.

UNIT–V: Application Porting,Building and Debugging

Porting Applications, Architectural Comparison, Application Porting Roadmap, Programmingwith Pthreads (only function names), OSPL definition, Building and Debugging in Linux (only overview).

Text Books

1. P Raghvan, Amol Lad, SriramNeelakandan, “Embedded Linux System Design and Development”, Auerbach Publications.

Reference Books

1. KarimYaghmour, Jon Masters, Gilad Ben-Yossef, and Philippe Gerum, “Building Embedded Linux Systems” O’Reilly publications, 2nd edition.
2. Christopher Hallinan, “Embedded Linux Primer: A Practical Real World Approach”, Prentice Hall, 2nd Edition, 2010.
3. Derek Molloy, “Exploring BeagleBone: Tools and Techniques for Building with Embedded Linux”, Wiley, 1st Edition, 2014.

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Professional Elective - II

PARALLEL PROCESSING

I Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with Implementation of pipelining and pipelining techniques.
- To develop parallel programming techniques.

Course Outcomes

Upon successful completion of the course, the students will be able to

- identify limitations of different architectures of computer
- analyze quantitatively the performance parameters for different architectures
- investigate the issues related to parallel programming development.

Course Content

UNIT–I: Overview

Over view of Parallel Processing and Pipelining, Performance metrics and measures, Scalability metrics, research issues and solutions.

UNIT–II: Advanced Processor Technology

Design space of processors, Instruction set architectures,CISC and RISC scalar processors, VLIW architecture, super scalar, vector and symbolic processors.

UNIT–III: Pipelining Techniques

Linear pipeline processors: Asynchronous and synchronous models, clocking and timing control, speedup efficiency, and throughput. Non linear pipeline processors: reservation and Latency analysis, collision free scheduling, pipeline schedule optimization.

UNIT–IV: Multithreading

Latency hiding techniques, Principles of multithreading, Issues and solutions, Multi dimensional architectures, Multicontext processors.

UNIT–V: Parallel Program Development

Message passing program development, Synchronous and asynchronous message passing.

Domain Decomposition, Control decomposition techniques, Heterogeneous processing.

Text Books

1. KaiHwang, Nareshjotwani, “Computer Architecture Parallelism, scalability, programmability”, MGH second edition. (Unit I – Unit V).
2. V. Rajaraman, L. Sivaram Murthy, “Parallel Computers”, PHI.

Reference Books

1. William Stallings, “Computer Organization and Architecture, Designing for performance “Prentice Hall, Sixth edition.
2. Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing”, MGH International Edition.
3. David Harris and Sarah Harris, “Digital Design and Computer Architecture”, Morgan Publishers.

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RESEARCH METHODOLOGY & IPR

I Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To impart the importance of research & IPR in professional growth.

Course Outcomes

Upon successful completion of the course, the students will be able to

- analyze various research methodologies
- perform research design
- collect and analyze the data required for research
- able to write research reports
- apply for Patents, Designs, Trade and Copyright.

Course Content

UNIT–I: Introduction

Research Methodology: Meaning of Research – Objectives – Types – Research Approaches – Significance of Research - Research Methods versus Methodology – Research and Scientific Method – Research Process – Criteria of Good Research – Research Ethics – Problems Encountered by Researchers in India.

Defining the Research Problem: What is a Research Problem? – Selecting the Problem – Necessity of Defining the problem – Technique Involved in Defining a Problem – An Illustration – Conclusion.

UNIT–II: Research Design

Meaning of Research Design – Need for Research Design – Features of a Good Design – Important Concepts Relating to Research Design – Different Research Designs – Basic Principles of Experimental Designs – Important Experimental Designs – Conclusion.

UNIT–III: Data Collection & Preparation, Report Writing

Data Collection: Introduction – Experiments and Surveys – Collection of Primary Data – Collection of Secondary Data – Selection of Appropriate Method for Data Collection – Case Study Method

Data Preparation: Data Preparation Process – Some Problems in Preparation Process – Missing Values and Outliers – Types of Analysis – Statistics in Research

Report Writing: Significance of Report Writing – Difference Steps in Writing Report – Layout of the Research Report – Types of Reports – Oral Presentation – Mechanics of Writing a Research Report – Precautions for Writing Research Reports - Conclusion.

UNIT–IV: Nature of Intellectual Property

Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT–V: Patent Rights & Developments

Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

Text Books

1. Kothari C.R "Research Methodology-Methods and Techniques",New age international Publishers, New Delhi.
2. T. Ramappa, "Intellectual Property Rights in India"

Reference Books

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students".
2. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.

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CMOS VLSI DESIGN LAB

I Semester

Practical	: 4	Internal Marks	: 30
Credits	: 2	External Marks	: 70

Course Objectives

- To familiarize with the design, simulation, power &timing analysis for various analog and digital circuits using EDA tool.

Course Outcomes

Upon successful completion of the course, the students will be able to

- use EDA tools.
- design, draw layout, perform simulation, power and timing analysis for analog and digital circuits.
- make oral presentations and prepare written reports.

List of Experiments:

Part A: For the following experiments, Design, Schematic entry/ Simulation/ Layout/ DRC/PEX/Post layout simulation/GDS-II are to be performed using CMOS devices.

1. Inverter
2. Universal gates using dynamic CMOS logic
3. Adder
4. Dynamic Latch
5. Register

Part B: The following experiments are to be designed using CMOS devices and simulation, power, timing analysis are to be performed.

1. CS amplifier with current mirror load
2. Cascode amplifier
3. Two-stage op-amp
4. Switched capacitor
5. Sampling switch

Part C: Open Ended Experiment – Design of Combinational/sequential circuit for achieving high speed/low power

Reference Books

1. Michael D. Ciletti, “Advanced Digital Design with the VERILOG HDL, 2nd Edition, Pearson Education, 2010.
2. R. Jacob Baker, “CMOS: Circuit Design, Layout, and Simulation”, IEEE Press, Wiley, 2010.

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ADVANCED MICROCONTROLLERS LAB

I Semester

Practical	: 4	Internal Marks	: 30
Credits	: 2	External Marks	: 70

Course Objectives

- To familiarize with interfacing 8051 with various I/O.
- To familiarize with embedded system design using Zynq SoC board.

Course Outcomes

Upon successful completion of the course, the students will be able to

- develop C programs to interface 8051 microcontroller to various I/O devices.
- design and develop embedded systems using Zynq SoC board.

List of Experiments:

PART-A: Write C programs to interface 8051 chip to Interfacing modules to develop single chip solutions.

1. Microcontroller interfaced with display devices.
2. External ADC and Temperature control interface to 8051.
3. Generate different waveforms Sine, Square, Triangular, Ramp etc. using DAC interface to 8051; change the frequency and amplitude.
4. Stepper and DC motor control interface to 8051.
5. Elevator interface to 8051.

PART-B: Perform Embedded System design using Zynq SoC board - Configuring Cortex processor on Zynq board using Xilinx Vivado.

1. Traffic signal controller
2. Digital clock

PART-C: Open ended Experiment

Text Books

1. Ajay V Deshmukh, "Microcontrollers-Theory and Applications", TMH Publications, 1st Edition, 2005.
2. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition.
3. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication.
4. https://www.xilinx.com/products/boards-and-kits/device-family/nav-zynq-7000.html

Reference Books

1. M. Ali Mazidi and J. Gillispie Mazidi , "The 8051 Microcontroller and Embedded Systems Using Assembly and C", 2nd Edition.
2. Lucio Bi Jasio, "PIC Microcontrollers", Newnes Publishers, 1st Edition, 2008.
3. Technical references and user manuals on www.arm.com.

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Audit Course - I

CONSTITUTION OF INDIA

I Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To understand the structure of Executive, Legislature and Judiciary.
- To understand the autonomous nature of Constitutional bodies like Supreme Court and High court controller and Auditor general of India and Election Commission of India.
- To understand the Central and State relation financial and administrative.

Course Outcomes

Upon successful completion of the course, the students will be able to

- apply the knowledge on Fundamental Rights and Duties and Directive principles of state policy.
- explain the role of President and Prime Minister and also know the Structure of Supreme court and High court.
- understand the Structure of State Government and also analyze the role of Governor and Chief Minister.
- compare and Contrast District administration role and importance.
- evaluate the various commissions of viz., SC/ST/OBC and Women.

Course Content

UNIT–I:

History of Making of the Indian Constitution: Sources. Features – Citizenship, Preamble, Fundamental Rights and Duties, Directive principles of State Policy.

UNIT–II:

Union Government and its administration Structure of the Indian Union: Federalism – Centre – state relationship. President: Role, power and position. Prime Minister and Council of ministers. Loksabha, Rajyasabha The Supreme Court and High Court: Powers and Functions.

UNIT–III:

State Government and its Administration Governor – Role and Position – Chief Minister and Council of ministers.

UNIT–IV:

Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation, Pachayati raj: Functions, PRI: ZilaPachayat. Elected offi-

cials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT–V:

Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

Text Books

1. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.
2. Subash Kashyap, Indian Constitution, National Book Trust.
3. J.C.Johari, Indian Government and Politics Hans.
4. H.M.Sreevani, Constitutional Law of India, 4th edition in 3 Volumes (Universal Law of Publication).

Reference Books

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.

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VLSI SYSTEM DESIGN

II Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with architecture of various Processors and Memory, Arithmetic Circuit Design.
- To introduce Clock, Reset Circuits and RAM modelling using VHDL programming language.

Course Outcomes

Upon successful completion of the course, the students will be able to

- understand the Architecture of various Processors and memory, arithmetic circuit design.
- program the clock, reset and RAM circuits.

Course Content

UNIT–I: Design of Memories

On-chip dual address ROM design, Single Address ROM Design, On-chip dual address RAM design, External Memory Controller Design.

UNIT–II: Arithmetic Circuit Design

Digital Pipelining, Partitioning of a design, Signed adder design-serial and parallel adder design, Multiplier design.

UNIT–III: Architectural Design

Architecture of Discrete Cosine Transform and Quantization Processor, Architecture of a video Encoder using automatic quality control scheme and DCTQ processor, Architecture for the FOSS motion estimation processor.

UNIT–IV: Clock and Reset Circuits

Clock buffer and clock tree, Clock tree generation, Reset circuitry, Clock skew and fixes, Synchronization between clock domains, Clock divider, Gated clock. M.Tech – VLSI Design and Embedded Systems (ECE) –R19 43.

UNIT–V: Dual –Port RAM, FIFO and DRAM Modelling

Dual-Port RAM, Synchronous FIFO, Asynchronous FIFO, Dynamic Random Access Memory.

Text Books

1. S.Ramachandran, “Digital VLSI Systems Design-A Design Manual for Implementation of Projects on FPGAs and ASICs using Verilog”, Springer International Edition, 2011. (Units: I to III)
2. K.C.Chang “Digital Systems Design with VHDL and Synthesis: An Integrated Approach” Wiley India Pvt. Ltd., New Delhi, 2009. (Units: IV,V) .

Reference Books

1. John F.wakerly “Digital Design: Principles & Practices” Pearson Education, 2006.
2. Samir Palnitkar “Verilog HDL: A Guide to Digital Design and Synthesis”, Prentice Hall PTR Publisher, Second Edition, 2003.

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EMBEDDED SYSTEM BASED IOT

II Semester

Lecture	: 3	nternal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To introduce the concepts of Embedded system hardware and software.
- To familiarize with Embedded System Design and IoT development.

Course Outcomes

Upon successful completion of the course, the students will be able to

- understand the concepts of embedded system with IoT.
- identify hardware and software requirements for an IoT system.
- design an embedded system applications using IoT.

Course Content

UNIT–I: Introduction

An embedded system-definition, examples, embedded system design flow, hardware design concepts, software development, processor in an embedded system and other hardware units, introduction to processor based embedded system design concepts.

UNIT–II: Embedded Hardware and Software

Embedded hardware building blocks, embedded processors – ISA architecture models, internal processor design, processor performance, Embedded operating systems –Multitasking and process management, memory management, I/O and file system management, OS standards example – POSIX, OS performance guidelines.

UNIT–III: Introduction to Internet of Things

Introduction to Internet of Things, Physical Design of IoT, Logical Design of IoT, IoT Enabling Technologies, IoT Levels.

UNIT–IV: IoT and M2M

M2M, Difference between IoT and M2M, SDN and NFV for IoT, Software defined Networking, Network Function Virtualization, Developing Internet of Things : Introduction, IoT Design Methodology, case study on IoT system for weather monitoring.

UNIT–V: IoT Systems - Logical Design using Python

Introduction, Python Data Types & Data Structures, Control Flow, Functions, Modules, Packages, File Handling, Date/ Time Operations, Classes, Python Packages. Introduction to IoT Device, Exemplary Device, Board, Linux on Raspberry Pi, Interfaces, and Programming & IoT Devices.

Text Books

1. Tammy Noergaard, "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier (Singapore) Pvt. Ltd. Publications, 2005. (Units - I, III)
2. Vijay Madisetti and Arshdeep Bahga, "Internet of Things (A Hands-on-Approach)", 1st Edition, VPT, 2014. (Units - IV,V)

Reference Books

1. Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & Sons Inc., 2002. (Unit - II).
2. Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos, David Boyle, "From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence", 1st Edition, Academic Press, 2014.

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Professional Elective - III

ADVANCES IN VLSI DESIGN

II Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with the current IC technologies, SOI MOSFETs, memristors, memories, reversible and adiabatic logic circuits.
- To acquaint with the power reduction, testing, yield, and packaging techniques, and verify the robustness of nanometer CMOS designs.

Course Outcomes

Upon successful completion of the course, the students will be able to

- understand the basic operation of CCD and CMOS image sensors, BICMOS circuits, power MOSFETs, SOI MOSFETs, memristors, reversible and adiabatic logic circuits.
- model multi-gate FETs
- distinguish working of various types of memories
- analyze power reduction, testing, yield, packaging techniques
- verify clocking, critical timing, signal integrity, variability, and reliability of nanometer scale CMOS circuit designs.

Course Content

UNIT – I: Special Circuits, Devices and Technologies

CCD and CMOS image sensors, BICMOS circuits, power MOSFETs, bipolar-CMOS-DMOS(BCD) processes, SOI MOSFET-MOSFET scaling and Moore's law, short-channel effects, gate geometry and electrostatic integrity, brief history of multiple-gate MOSFETs, framework for multi-gate FET modeling, multi-gate BSIM-CMG and BSIM-IMG models; Memristors-introduction, working of memristance, resistance to memristance, axiomatic definition of circuit elements.

UNIT – II: Memories

Introduction, serial memories, content-addressable memories, random-access memories, non-volatile memories, embedded memories.

UNIT – III: Power Reduction Techniques, Testing, Yield, and Packaging

Battery technology, sources of power consumption, technology options for low power, design options for power reduction, testing, yield, packaging.

UNIT – IV: Robustness of Nanometer CMOS Designs

Clock generation, clock distribution and critical timing, signal integrity, variability, reliability.

UNIT – V: Fundamentals of Reversible and Adiabatic Logic Circuits

Fundamental concepts of reversible logic, a brief history of reversible computation and adiabatic logic, fundamentals of adiabatic logic - the charging process in adiabatic logic compared to static CMOS, an adiabatic system, loss mechanisms in adiabatic logic, voltage scaling, properties of adiabatic logic and resultant design considerations.

Text Books

1. Harry J.M. Veendrick, "Nanometer CMOS ICs: From Basics to ASICs", Springer International Publishing, AG 2017, Second Edition (Units: I – IV).
2. Jean-Pierre Colinge (Ed.), "FinFETs and Other Multi-Gate Transistors", Springer Series on Integrated Circuits and Systems, 2008 (Unit: I).
3. Ronald Tetzlaff (Ed.), "Memristors and Memristive Systems", Springer Science, 2014 (Unit: I).
4. Ashutosh Kumar Singh, Masahiro Fujita, and Anand Mohan (Eds.), "Design and Testing of Reversible Logic", Springer Lecture Notes in Electrical Engineering, Volume 577, 2020 (Unit: V).
5. Philip Teichmann, "Adiabatic Logic: Future Trend and System Level Perspective", Springer Series in Advanced Microelectronics, 2012 (Unit: V).

Reference Books

1. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, "Digital Integrated Circuits-A Design Perspective", Prentice Hall Inc., 2nd Edition, 2003.
2. Neil H.E.Weste and David Money Harris, "CMOS VLSI Design: A Circuits and Systems Perspective, Addison-Wesley, 4th Edition, 2011.
3. Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", McGraw-Hill International 3rd Edition, 2003.

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Professional Elective - III

EMBEDDED COMPUTER ARCHITECUTERS

II Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with embedded platform, processor architectures and power optimization techniques.
- To impart the knowledge of VLIW and ISA Architectures.

Course Outcomes

Upon successful completion of the course, the students will be able to

- understand embedded platform and processor architectures.
- make intelligent choices between hardware/software tradeoffs.
- analyze different power optimization techniques in processor architectures.
- develop an embedded system with VLIW, ISA Architectures.
- understand embedded processing in automotive and Hard disk drives Applications.

Course Content

UNIT–I: Embedded Platform Architecture

Embedded platform overview and characteristics, volatile memory technologies, non- volatile storage, device interface-high performance, universal serial bus, device interconnect – low performance; general purpose input/output, power delivery.

UNIT–II: Embedded processor Architecture

Basic execution environment, application binary interface, processor instruction classes, exceptions/interrupts model, vector table structure, exception frame, masking and acknowledging interrupts, interrupt latency, memory mapping and protection, MMU and processes, memory hierarchy, Intel atom micro architecture.

UNIT–III: Power Optimization

Basics, power profile of an embedded computing system, constant versus dynamic power, simple model of power efficiency, advanced configuration and power interface, optimizing software for power performance.

UNIT–IV: Overview of VLIW and ISA

Semantics and Parallelism, Design Philosophies, VLIW in the Embedded and DSP Domains, Basic VLIW Design Principles, Designing a VLIW ISA for Embedded Systems.

UNIT–V: Application Areas

Automotive- Fail-safety and Fault Tolerance, Engine Control Units, Hard disk drives- Motor Control, Data Decoding, Disk Scheduling and on/off -disk Management.

Text Books

1. Peter Barry and Patrick Crowley, "Modern Embedded Computing", 1st Edition, Elsevier/Morgan Kaufmann, 2012.(Units I to III).
2. Joseph A.Fisher, Paolo Faraboschi, Cliff Young, "Embedded computing: a VLIW approach to architecture, compilers and tools", Elsevier/ MorganKaufmann, 2005. (Units IV and V).

Refernce Books

1. DezsoSima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architectures", Pearson Education Ltd, 2002.
2. Kai Hwang, "Advanced computer architecture –Parallelism, Scalability Programmability",McGraw Hill, 1993.

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Professional Elective - III

SYSTEM ON CHIP DESIGN

II Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with the concept of System-On-Chip design technology.
- To introduce components in a typical SoC system.
- To familiarize with the concept of different processor cores.

Course Outcomes

Upon successful completion of the course, the students will be able to

- understand architecture, design issues, core libraries and EDA tools required for SoC design.
- understand design methodology for logic cores, soft and hard cores, memory and analog cores.
- perform SoC design validation, prototyping and verification.

Course Content

UNIT–I: Introduction to Architecture Designs

Architecture and design issues of SoC, hardware software co-design, co-design flow, core libraries, EDA tools and web pointers.

UNIT–II: Design Methodology for Logic Cores, Soft and Firm Cores

Logic Cores: SoC design flow, guidelines for design reuse and physical design. Soft and Firm Cores: Soft core design flow, design process for hard cores, sign-off checklist, deliverables and system integration.

UNIT–III: Design methodology for Memory Cores and Analog Cores

Memory Cores: Embedded memories and design methodology, specifications of analog circuits, circuit techniques, memory compiler, simulation models.

Analog Cores: Analog-to-digital converter, digital-to-analog converter, phase-locked loops, high speed circuits

UNIT–IV: Design Validation

Core-level validation, core validation plan, test benches, core-level timing verification, core interface verification, protocol verification, gate-level simulation, SoC design validation, co-simulation, emulation, hardware prototypes.

UNIT–V: Core Design Examples

Micro processor cores, V830 R/AV super scalar RISC core, design of power PC603e G2 core, memory core generators, core integration and on-chip bus.

Text Books

1. Rochit Raj Suman, “System-on-a-chip: Design and Test”, Artech House, 2000.

Reference Books

1. Jason Andrews – Newness “Co-Verification of Hardware and Software forARM System on Chip Design (Embedded Technology) “, BK and CDROM.
2. Prakash Rashinkar, Peter Paterson and Leena Singh L “System on ChipVerification – Methodologies and Techniques”, Kluwer Academic Publishers,2001.
3. Ricardo Reis,”Design of System on a Chip: Devices and Components”, 1st Ed., Springer 2004.

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Professional Elective - IV

VLSI INTERCONNECTS

II Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To impart with interconnect issues, parameters and models.
- To familiarize with the concepts of crosstalk effects and advanced interconnect techniques.

Course Outcomes

Upon successful completion of the course, the students will be able to

- describe different types of interconnect models.
- analyse the role of capacitive and resistive parasitics in system performance
- estimate the delay and energy dissipation due cross talk and gain knowledge of cross talk effects.
- apply various techniques to avoid interconnect noise and advanced interconnects.

Course Content

UNIT–I: Interconnects and Wire models

Interconnect Parameters: Resistance, Inductance, and Capacitance, Interconnect RC Delays, Interconnect Models: The ideal wire, The lumped RC Model, the distributed RC Model, the transmission line model.

UNIT–II: Coping with Interconnect

Capacitive Parasitics: Capacitance and Reliability, Capacitance and Performance in CMOS; Resistive Parasitics: Resistance and Reliability— Ohmic Voltage Drop, Electromigration, Resistance and Performance.

UNIT–III: Crosstalk effects

Cross talk induced delay, Energy dissipation due to crosstalk: Model for energy calculation of two coupled lines. Contribution of driver and interconnect to dissipated energy, Crosstalk effects in logic VLSI circuits: Static circuits, Dynamic circuits and various remedies.

UNIT–IV: Techniques for Avoiding Interconnection Noise

Cross talk avoidance: Technology Solution, Interconnection Layout, Driver Sizing, Tolerant circuits; Switching Noise Avoidance: Package Technology, Use of Capacitors, Pin Assignment, Circuit Techniques.

UNIT–V: Advanced Interconnect Techniques

Reduced-swing Circuits: Static Reduced-Swing Networks, Dynamic Reduced-Swing Networks Current-mode Transmission Techniques.

Text Books

1. Jan M. Rabaey, "Digital Integrated Circuits– A design Perspective", Tata McGraw-Hill Education, 2nd Edition, 2003. (Unit – I, II, V).
2. F.Moll, M.Roca, "Interconnection Noise in VLSI Circuits", Kluwer Academic Publishers-2004 Springer (Units - III, IV).

References Books

1. Ashok K. Goel, "High-Speed VLSI Interconnects", 2nd Edition, IEEE Press, Wiley-Interscience publication, 2007.
2. David Hodges, "Analysis and Design of Digital Integrated Circuits", Tata McGraw-Hill Education, 3rd Edition, 2005.
3. Y.S. Diamand, "Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications", 2009
4. H.S Philip Wong and Deji Akinwande, "Carbon nanotube and Graphene Device Physics", 2011.
5. Bakoglu H. B., "Circuit Interconnect and Packaging for VLSI", Addison-Wesley, 1st Edition, 1990.

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Professional Elective - IV

COMMUNICATION BUSES AND INTERFACES

II Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with the concepts of Serial and Parallel Buses.
- To gain in-depth knowledge of USB and CAN buses.

Course Outcomes

Upon successful completion of the course, the students will be able to

- distinguish serial and parallel buses communication protocols.
- analyze various evolutions of USB interface.
- interface USB 2.0 with embedded processors.
- discriminate various frames in MAC layer of CAN bus.
- apply the CAN bus controllers for different microcontrollers.

Course Content

UNIT – I: Introduction

IO Types and Examples, Serial Communication Devices, Serial Bus Communication Protocols, Parallel Bus Communication Protocols.

UNIT – II: USB Basics and Transfers

USB Basics - Evolution of an USB interface, Bus components; Inside USB Transfers - Transfer basics, Elements of a transfer, USB 2.0 transactions, Ensuring successful transfers.

UNIT – III: USB Enumeration, Descriptors, Components and Hosts

Enumeration-Events and requests-Getting to the Configured state; Descriptors-Types; Chip Choices-Components of a USB device, USB microcontrollers-Microchip PIC18; How the Host Communicates-Device drivers; Hosts for Embedded Systems- The Targeted Host;

UNIT – IV: CAN Bus Concepts and Definitions

Concepts of bus access and arbitration, Error processing and management, From Concept to Reality- Introduction to CAN, The CAN offer: a complete solution; Definitions of the CAN protocol.

UNIT – V: Components, Applications and Tools for CAN

CAN Components- General architecture and functional division of CAN components, List of existing component types, Microcontrollers with integrated CAN handlers: the 8xC592; Applications- Physical and functional divisions of a CAN-based system, CAN central unit with SJA 1000.

Text Books

1. Raj Kamal, “Embedded Systems– Architecture, Programming and Design”, McGraw-Hill Education (India) Pvt. Ltd., 2nd Edition, 2013. (Unit – I).
2. Jan Axelson, “USB Complete”, 5th Edition, Lakeview Research, 2014. (Units - II, III)

References Books

1. Dominique Paret, “Multiplexed Networks for Embedded Systems”, John Wiley & Sons Ltd., 2007. (Units - IV, V)
2. Jan Axelson, “Serial Port Complete”, 2nd Edition, Lakeview Research, 2007.
3. Wilfried Voss, Copperhill Media, “A Comprehensive Guide to controller Area Network –Corporation”, 2nd Edition, 2005.

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Professional Elective - IV

ADVANCED DIGITAL SIGNAL PROCESSING

II Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with concepts of different types of filter banks and structures.
- To f amiliarize with different adaptive algorithms and its applications on various fields.

Course Outcomes

Upon successful completion of the course, the students will be able to

- understand the fundamentals of multirate signal processing and its applications.
- design perfect reconstruction filter bank system.
- understand the fundamentals of adaptive systems and its applications.

Course Content

UNIT–I: Basic Multirate Operations

Decimation and interpolation, time-domain characterization, frequency-domain characterization, cascade equivalences, filters in sampling rate alteration systems, polyphase decomposition.

UNIT–II: Filter Banks

Digital filter banks- uniform DFT filter banks, polyphase implementation of uniform filter banks, nyquist filters. two channel Quadrature-Mirror Filter (QMF) bank-filter bank structure, analysis of two channel QMF bank, alias free filter bank, alias free realization, alias free FIR QMF bank, alias free IIR QMF bank, perfect reconstruction two channel QMF bank.

UNIT–III: Adaptive Systems

Adaptive systems- definitions and characteristics- properties, adaptive linear combiner-input signal and weight vectors - performance function-gradient and minimum mean square error.

UNIT–IV: Adaptive Algorithms

Searching performance surface-stability and rate of convergence - learning curve-gradient search - Newton's method - method of steepest descent – comparison. LMS algorithm- convergence of weight vector. The LMS/Newton algorithm.

UNIT – V: Applications of Adaptive Systems

Applications-adaptive modeling and system identification-adaptive modeling for multipath communication channel, geophysical exploration, FIR digital filter synthesis.

Text Books

1. Sanjit K. Mitra, " Digital Signal Processing: A computer based approach", McGraw Hill, 1998. (Units – I, II).
2. Bernard Widrow and Samuel D. Stearns, "Adaptive Signal Processing", Pearson Education, 2005. (Units – III, IV, V).

Reference Books

1. P.P. Vaidyanathan, "Multirate Systems and Filter Banks." Prentice Hall.PTR. 1993.
2. Simon Haykin, "Adaptive Filter Theory", Pearson Education, 2003.
3. J.G. Proakis. D.G. Manolakis. "Digital Signal Processing: Principles.Algorithms and Applications", 3rd Edn. Prentice Hall India, 1999.
4. N.J. Fliege. "Multirate Digital Signal Processing " John Wiley 1994.

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VLSI SYSTEM DESIGN LAB

II Semester

Practical	: 4	Internal Marks	: 30
Credits	: 2	External Marks	: 70

Course Objectives

- To design, simulation, power & timing analysis for various analog and digital circuits using EDA tool.

Course Outcomes

Upon successful completion of the course, the students will be able to

- use EDA tools.
- design, simulate, synthesize, test, and analyze various digital circuits
- design, draw layout, perform simulation, power and timing analysis for analog and digital circuits.
- make oral presentations and prepare written reports.

List of Experiments:

For the following experiments, specifications, design entry using HDL, logic simulation using test bench, RTL logic synthesis, post synthesis timing simulation, place & route, design for testability, static timing analysis, power analysis are to be performed and should be implemented in FPGA.

1. Analysis of 4-bit carry select adder, carry skip adder, carry look adder.
2. CRC-4 encoder
3. Power dissipation calculation for (8bit, 16bit, 32 bit) LFSR using BIST.
4. 8-bit ALU.
5. Multiplexed Display Controller (MDC).
6. MAC using filters.
7. Mealy/Moore sequence detector (with and without overlap).
8. FIFO and LIFO buffers.
9. Gate level analysis of different stuck-at - faults in a logic gate.
10. Clock Divider for 4-bit counter
11. Open Ended Experiment

Reference Books

1. Michael D. Ciletti, “Advanced Digital Design with the VERILOG HDL, 2nd Edition, Pearson Education, 2010.
2. R. Jacob Baker, “CMOS: Circuit Design, Layout, and Simulation”, IEEE Press, Wiley, 2010.

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EMBEDDED SYSTEMS AND IOT LAB

II Semester

Lecture	: 4	Internal Marks	: 30
Credits	: 2	External Marks	: 70

Course Objectives

- To familiarize with the high level language programming and I/O interfacing of ARM/FPGA/DSP.
- To familiarize with the edge device concepts in IoT.

Course Outcomes

Upon successful completion of the course, the students will be able to

- perform I/O interface with ARM/FPGA Processor.
- execute various signal processing operations using python script and different IoT protocols.
- make oral presentations and prepare written reports.

List of Experiments:

Note: Any four experiments from Part-1 and any three from Part-2 are to be performed.

Part - 1: The following experiments are to be implemented using High level language programming and porting it on ARM/FPGA/DSP processor.

1. Reading data from cloud
2. Read data from a sensor and process using Cloud
3. Real time Data Acquisition Implementation
4. Perform DSP operations (FFT/DCT/DWT) on HARDWARE
5. Design and implementation of the Real-time SoC using Xilinx IP cores.

Part - 2: The following experiments are to be implemented using Python/Arduino Script and different IOT protocols

Hardware: ARM Embedded board, software Programming: Python.

1. Reading switch status and display it on LED.
2. Interfacing an ultrasonic sensor to an IoT device.
3. Interfacing any two sensors and send data to cloud with MQTT protocol.
4. Home Automation– sending an e-mail/SMS.
5. Air pollution monitoring system using gas sensors (CO & NO2).
6. Running web server on Raspberry pi.
7. Communicate multiple devices over socket.

Part - 3: Open ended experiment - IOT based smart system.

Reference Books

1. Stephen B Furber, "ARM System on Chip Architecture", Pearson Publications, 2nd Edition.
2. G. John Proakis and G. Dimitris Manolakis, "Digital Signal Processing, Pearson Education", 4th edition.
3. Vijay Madisetti, Arshdeep Bahga," Internet of Things: A Hands-On- Approach", 2014.
4. https://www.xilinx.com/support/documentation/data.../ds190-Zynq-7000.
5. Cloud access: https://thingspeak.com/channels.
6. https://www.mathworks.com/help/thingspeak.

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Audit Course - II

ENGLISH FOR RESEARCH PAPER WRITING

II Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To equip the trainees with the critical thinking skills required for crafting research issues into researchable questions.
- To develop in them research paper writing skills in three areas – vocabulary, discourse, and style;
- To enhance their awareness of the referencing conventions vis-à-vis scholarly communication;
- To develop in them an understanding of the knowledge-constructing practices of their disciplines (under the guidance of a research mentor on an apprenticeship programme) and sharpen that understanding so as to enable them to identify research issues, investigate them, and then present and publish papers on them.

Course Outcomes

Upon successful completion of the course, the students will be able to

- craft research issues into researchable questions;
- write appropriate introductions and conclusions to academic / research texts;
- review research literature using the skills of analysis, synthesis, critical evaluation, paraphrasing, and summarising and avoiding the risk of plagiarism;
- use the right vocabulary for different research communication purposes, such as stating study aims, reviewing sources, describing research designs, presenting arguments, evaluating and emphasizing, and analysing and discussing results.
- organise texts following the discourse rules of coherence and cohesion;
- write research paper abstracts; and
- communicate their research in academic style with grammatical accuracy.

Course Content

UNIT–I:

Understanding Researchability: Evaluating research questions in order to gain awareness of researchability - Identifying research issues, developing research questions from them, and crafting them into researchable questions

Academic Vocabulary: Neutral, and formal vocabulary - Nominalisation - Phrases commonly used in research communication

UNIT–II:

Writing and Rhetorical Conventions: Writing introductions - Writing conclusions - Discourse organization

Academic Vocabulary: Research and Study aims.

UNIT–III:

Writing and Rhetorical Conventions: Summarising - Paraphrasing -

Academic Vocabulary: Evaluating and critiquing

UNIT–IV:

Writing and Ahetorical Conventions: Writing abstracts - Varying sentence length and structure

Remedial Grammar

UNIT–V:

Writing and Rhetorical Conventions: Avoiding repetition and redundancy - Style of academic / scholarly communication - Referencing

Academic Vocabulary: Analysing and discussing results

Apprenticeship

The apprenticeship will involve each individual trainee, under the guidance of a research mentor in his/her department, developing and crafting research questions on issues of his/her concern, investigating at least one of those issues during the course of the internship, and writing a paper on it which, before its presentation or publication, will be reviewed or assessed, as part of the internal assessment, by a panel of experts in the trainees' own departments. The entire process could be broken down into the following skills:

a. Identifying research issues
b. Framing the issues – developing research questions from them, refining them, and crafting them
c. Addressing literature
d. Investigating one of those issues by selecting an appropriate research design and data collection procedures and arriving at conclusions
e. Gaining competence in disciplinary specialized discourse conventions
f. Presenting arguments which scholars anticipate
g. Writing a paper on the study, presenting it before a panel of experts, and revising the paper on the basis of feedback from the panel
h. Determining the prestige of journals
i. Establishing a paper-journal fit and submitting the revised paper for publication
j. Learning to negotiate two principal audiences in one's scholarly communication – the community of scholars and journal gate-keepers
k. Negotiating peer review and editorial commentary

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Professional Elective - V

LOW POWER VLSI DESIGN

III Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To make the students to gain in depth knowledge with the sources of power dissipation and power minimization techniques.
- To make them familiarize with advanced low power design techniques

Course Outcomes

Upon successful completion of the course, the students will be able to

- describe the requirements for low power and distinguish static and dynamic power dissipations
- apply voltage scaling approaches to reduce dynamic power
- apply various techniques to minimize switched capacitance
- identify suitable leakage power minimization technique
- analyze modern low power design methodologies such as adiabatic circuits.

Course Content

UNIT–I: Low Power Requirements and Sources of Power Dissipation

Historical background, requirements for low power, sources of power dissipation, low power design methodologies, Short circuit power dissipation, switching power dissipation, glitching power dissipation, leakage power dissipation.

UNIT–II: Supply Voltage Scaling Approaches

Device feature size scaling, architectural level approaches, voltage scaling using high-level transformations, multilevel voltage scaling.

UNIT–III: Switched Capacitance Minimization Approaches

Hardware software trade-off, bus encoding, clock gating, glitching power minimization, logic styles for low power.

UNIT–IV: Leakage Power Minimization Approaches

Variable-Threshold voltage CMOS (VTCMOS) approach, transistor stacking, Multi-Threshold-voltage CMOS (MTCMOS) approach, power gating.

UNIT – V: Adiabatic Logic Circuits

Adiabatic charging, adiabatic amplification, adiabatic logic gates, pulsed power supply, partially adiabatic circuits.

Text Books

1. Jan M. Rabaey and Massoud Pedram, “Low Power Design Methodologies”, Kluwer Academic Publishers, 1996 (Unit - I).
2. Ajit Pal, “Low Power VLSI Circuits and Systems”, Springer India, 2015. (Units - II to V).

Reference Books

1. Sung Mo Kang and Yusuf Leblebici, “CMOS Digital Integrated Circuits”, Tata Mcgraw Hill, Third Edition.
2. Neil H. E. Weste and K. Eshraghian, “Principles of CMOS VLSI Design”, Addison Wesley (Indian reprint), Second Edition.
3. A. Bellamour and M. I. Elmasri, “Low Power VLSI CMOS Circuit Design”, Kluwer Academic Press, 1995.
4. Anantha P. Chandrakasan and Robert W. Brodersen, “Low Power Digital CMOS Design”, Kluwer Academic Publishers, 1995.
5. Kaushik Roy and Sharat C. Prasad, “Low-Power CMOS VLSI Design”, Wiley-Interscience, 2000.
6. Prof. Ajit Pal, Department of Computer Science and Engineering, IIT Kharagpur, Low Power VLSI Circuits & Systems, NPTEL video course.

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Professional Elective - V

NETWORK SECURITY AND CRYPTHOGRAPHY

III Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with fundamentals of cryptography and its application to network security.
- To introduce the concept of Hash functions and IP security

Course Outcomes

Upon successful completion of the course, the students will be able to

- understand various Cryptographic Techniques
- apply various public key cryptography techniques.
- implement Hashing and Digital Signature techniques.
- understand the various types of Web Security.

Course Content

UNIT–I: Introduction & Symmetrical Ciphers

OSI Security architecture, Security attacks, Security services, Security Mechanisms, A Model for Internetwork security, Classical Techniques: Conventional Encryption model, Steganography ,Rotor Machines, symmetrical cipher model, substitution Techniques, transposition Techniques, Traditional Block Cipher structure, Block cipher Design Principles, Block cipher Operation.

UNIT–II: Classical Encryption Techniques

The Data Encryption Standard (DES), DES Example, the strength of DES, Advanced Encryption Standard(AES), AES structure, AES Transformation Functions, AES Example, AES Implementation, Multiple Encryption and Triple DES.

UNIT–III: Public Key Cryptography

Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography. Number Theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primarily, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

UNIT–IV: Message Authentication and Hash Functions

Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs. Hash and Mac Algorithms: MD File, Message digest Algorithm, Secure Hash Algorithm. Digital signatures and Au-

thentication protocols: Digital signatures, Authentication Protocols, Digital signature standards. Authentication Applications: Kerberos, Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT–V: IP Security

Overview, Architecture, Authentication, Encapsulating Security Payload, Key Management. Web Security: Web Security requirements, secure sockets layer and Transport layer security, Secure Electronic Transaction. Intruders, Viruses and Worms: Intruders, Viruses and Related threats. Fire Walls: Fire wall Design Principles, Trusted systems.

Text Books

1. William Stallings, "Cryptography and Network Security: Principles and Practice", 6th Edition, Pearson Education, 2013.
2. William Stallings, "Network Security Essentials (Applications and Standards)", 4th Edition, Pearson Education.

Reference Books

1. Terry D. Pardoe, Gordon Snyder, "Network Security", Thomson/Delmar Learning, 2005.
2. Behrouz A. Forouzan, Debdeep Mukhopadhyay, "Cryptography and Network Security (SIE)", Tata Mcgraw-Hill Education Private Limited, 2011.

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Open Elective

SUSTAINABLE DEVELOPMENT

III Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To help the students understand the fundamental key concepts on Sustainable Development (SD),suchasintra-andinter-generational equity, economic, social and environmental,sustainability, strong and weak sustainability, natural capitalism, steady state and green economy.
- To enable students to identify and discuss in detail the key empiricalissues on sustainable development, such as renewable energy transitions, urban agriculture and green architecture.
- To empower students with the expertise to distinguish between "greeneconomy" and "sustainability" and various efforts at multiple levels ofgovernance:from individual to governments.
- To exposestudents to awide varietyof research areas to apply and therefore appropriate the oretical knowledge on public policy and international relations to the issue area of sustainable development, insuch aspects as international aid, global climate change negotiations, the importance of international regimes as opposed to voluntary private governance.
- To empower Students to make their own lives more sustainable and join social movements to bring about more of sustainable development.

Course Outcomes

Upon successful completion of the course, the students will be able to

- gainknowledgeofsustainabilityandbiodiversity
- studyaboutgreenhousegases
- learndynamicsofsustainability
- gainKnowledgeonsocio-economicsystems
- studyabouttheconventionsonsustainabledevelopment
- learnconceptofSustainableDevelopmentanditsrolein buildingofenvironment

Course Content

UNIT–I: Concept of Sustainable Development

Definition of sustainability - History and emergence of the concept of Sustainable development – Our Common Future - Objectives of Sustainable Development - Millennium Development Goals - Environment and Development linkages – Globalization and environment - Population, Poverty and Pollution –Global, Regional

and Local environmental issues–Resource Degradation–Greenhouse gases and climate Change – Desertification – Industrialization –Socialinsecurity.

UNIT–II: Sustainability and thetriple bottom line

Components of sustainability–Complexity of growth and equity-Social, economic and environmental dimensions of sustainable development–Environment–Biodiversity–Natural Resources–Ecosystem integrity–Clean air and water–Carrying capacity–Equity, Quality of Life, Prevention, Precaution, Preservation and Public participation. - Structural and functional linking of developmental dimensions – Sustainability in national and regional context..

UNIT–III: Sustainable Development and International Response

Role of developed countries in the development of developing countries–International summits–Stock holm to Johannes burg–Rio Principles–Agenda 21-Conventions–Agreements–Tokyo Declaration-Doubling Statement - Trans boundary issues – Integrated approach for resource protection and management.

UNIT–IV: Sustainable Development of Socio-Economic Systems

Demographic dynamics of sustainability – Policies for socio-economic development –Strategies for implementing eco-development programmes – Sustainable development through trade – Economic growth – Action plan forimplementing sustainable development – Urbanization and Sustainable Cities –Sustainable Energy and Agriculture –Sustainable Livelihoods – Ecotourism.

UNIT–V: Framework for Achieving Sustainability

Sustainability indicators - Hurdles to Sustainability - Operational guidelines – Inter connected pre-requisites for sustainable development – Empowerment of Women, Children, Youth, Indigenous People, Non-Governmental Organizations, Local Authorities, Business and Industry-Science and Technology for sustainable development – Performance indicators of sustainability and Assessment mechanism – Constraints and barriers for sustainable development.

Text Books

1. Austin, James and Tomas Kohn. 1990. Strategic Management in DevelopingCountries.TheFreePress.
2. Berger. 1994. “The Environment and the Economy.” In Smelser and Swedberg(eds.)
3. TheHandbookofEconomicSociology.RusselSageFoundation.D’Arcy,David. Transcript of broadcast, Dec. 5, 2002, “In Houston, a Treasure of ExiledAfghanArt,”National PublicRadio,

Reference Books

1. Elkington, John. Cannibals with Forks:TheTriple Bottom Line for 21stCenturyBusiness Oxford:Capstone Publishing,October 1997.
2. Guillen, Mauro and Sandra L. Suarez. 2002. “The Institutional Context of Multinational Activity.”In Organization Theory and the Multinational Corporation” .2ndedition. New York: St.Martin’s Press.

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Open Elective

ENERGY AUDIT, CONSERVATION & MANAGEMENT

III Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To learn principle of energy audit as well as management for industries and utilities and buildings.
- To study the energy efficient motors and lighting.
- To learn power factor improvement methods and operation of different energy instruments.
- To compute depreciation methods of equipment for energy saving.

Course Outcomes

Upon successful completion of the course, the students will be able to

- understand the principle of energy audit and their economic aspects.
- recommend energy efficient motors and design good lighting system.
- understand advantages to improve the power factor.
- evaluate the depreciation of equipment.

Course Content

UNIT–I: Basic Principles of Energy Audit

Energy audit- definitions, concept , types of audit, energy index, cost index ,pie charts, Sankey diagrams and load profiles, Energy conservation schemes- Energy audit of industries- energy saving potential, energy audit of process industry, thermal power station, building energy audit.

UNIT–II: Energy Management

Principles of energy management, organizing energy management program, initiating, planning, controlling, promoting, monitoring, reporting. Energy manager, qualities and functions, language,Questionnaire – check list for top management.

UNIT–III: Energy Efficient Motors and Lighting

Energy efficient motors, factors affecting efficiency, loss distribution, constructional details, characteristics – variable speed , variable duty cycle systems, RMS - voltage variation-voltage unbalanceover motoring-motor energy audit. lighting system design and practice, lighting control, lighting energy audit.

UNIT–IV: Power Factor Improvement and Energy Instruments

Power factor – methods of improvement, location of capacitors, Power factor with non-linear loads, effect of harmonics on p.f, p.f motor controllers – Energy

Instruments- watt meter, data loggers, thermocouples, pyrometers, lux meters, tongue testers,application of PLC s.

UNIT–V: Economic Aspects and their Computation

Economics Analysis depreciation Methods, time value of money, rate of return, present worth method, replacement analysis, lifecycle costing analysis – Energy efficient motors. Calculation of simple payback method, net present value method-Power factor correction, lighting – Applications of life cycle costing analysis, return on investment.

Text Books

1. Energy management by W.R.Murphy&G.Mckay Butter worth, Heinemann publications, 1982.
2. Energy management hand book by W.CTurner, John Wiley and sons, 1982.

Reference Books

1. Energy efficient electric motors by John.C.Andreas, Marcel Dekker Inc Ltd-2nd edition,1995
2. Energy management by Paul o Callaghan, Mc-graw Hill Book company-1st edition, 1998
3. Energy management and good lighting practice : fuel efficiency- booklet12-EEO.

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Open Elective

RAPID PROTOTYPING

III Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with Rapid Prototype tools and techniques for design and Manufacturing.

Course Outcomes

Upon successful completion of the course, the students will be able to

- assess the need of RPT in Product development.
- use appropriate RT Software for development of Prototype model.
- judge the correct RP Process for Product/Prototype development.
- predict the technical challenges in 3D printing.
- list the applications of RPT.

Course Content

UNIT–I: Introduction to Rapid Prototyping

Introduction to prototyping, traditional prototyping Vs. rapid prototyping (RP), need for time compression in product development, usage of RP parts, generic RP process, distinction between RP and CNC, other related technologies, classification of RP.

UNIT–II: RP Software and Software Issues of RP

RP Software: Need for RP software, MIMICS, magics, surgiGuide, 3D-doctor, simplant, velocity2, voxim, solidView, 3Dview, etc., software.

Software Issues of RP: Preparation of CAD models, problems with STI, files, STL file manipulation, RP data formats: SLC, CLI, RPI, LEAF, IGES, HP/GL, CT, STEP.

UNIT–III: Photopolymerization RP Processes, Powder Bed Fusion RP Processes and Extrusion-Based RP Systems

Photopolymerization RP Processes: Sterolighography (SL), SL resin curing process, SL scan patterns, microstereolithography, applications of photopolymerization processes.

Powder Bed Fusion RP Processes: Selective laser sintering (SLS), powder fusion mechanism and powder handling, SLS metal and ceramic part creation, electron beam melting (EBM), applications of powder bed fusion processes.

Extrusion-Based RP Systems: Fused deposition modelling (FDM), principles, plotting and path control, applications of extrusion-based processes..

UNIT–IV: Printing RP Processes, Sheet Lamination RP Processes and Beam Deposition RP Processes

Printing RP Processes: 3D printing (3DP), research achievements in printing deposition, technical challenges in printing, printing process modeling, applications of printing processes.

Sheet Lamination RP Processes: Laminated Object Manufacturing (LOM), ultrasonic consolidation (UC), gluing, thermal bonding, LOM and UC applications.

Beam Deposition RP Processes: Laser Engineered Net Shaping (LENS), Direct Metal Deposition (DMD), processing – structure - properties, relationships, benefits and drawbacks.

UNIT–V: Rapid Tooling, Errors in RP Processes and RP Applications

Rapid Tooling: Conventional Tooling Vs. Rapid Tooling, classification of rapid tooling, direct and indirect tooling methods, soft and hard tooling methods.

Errors in RP Processes: Pre-processing, processing, post-processing errors, part building errors in SLA, SLS, etc.,

RP Applications: Design, engineering analysis and planning applications, rapid tooling, reverse engineering, medical applications of RP.

Text Books

1. Chua Chee Kai., Leong KahFai., Chu Sing Lim, “Rapid Prototyping: Principles and Applications in Manufacturing”, World Scientific

Reference Books

1. Ian Gibsn., David W Rosen., Brent Stucker., “Additive Manufacturing Technologies: Rapid Prototyping to Direct Digital Manufacturing”, Springer, 2010
2. Pham, D.T, Dimov, S.S, Rapid Manufacturing, Springer, 2001.

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Open Elective

AUTOMOTIVE ELECTRONICS

III Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To familiarize with the electronic systems inside automotive vehicle.
- To introduce with the concepts of advanced safety systems

Course Outcomes

Upon successful completion of the course, the students will be able to

- learn the fundamentals of automotive technology.
- describe the operation of microcomputer systems.
- acquire knowledge in automotive sensors and control systems.
- develop communications & navigation/routing in automotive vehicles.

Course Content

UNIT–I: Automotive Fundamentals

Use of electronics in the automobile, evolution of automotive electronics, the automobile physical configuration, evolution of electronics in the automobile, survey of major automotive systems, engine control or electronic control unit, ignition system.

UNIT–II: Automotive Micro-Computer System

Binary number system, binary counters, Microcomputer fundamentals-digital versus analog computers, basic computer block diagram, microcomputer operations, CPU registers, accumulator registers, condition code register-branching; microprocessor architecture, memory-ROM, RAM; I/O parallel interface, digital to analog converter and analog to digital converters with block diagram.

UNIT–III: Basics of Electronics Engine Control

Motivation for electronic engine control, exhaust emissions, fuel economy, concept of an electronic engine control system, engine functions and control, electronic fuel control configuration, electronic ignition with sensors.

UNIT–IV: Sensors and Actuators

Introduction; basic sensor arrangement; types of sensors such as oxygen sensors, crank angle position sensors, fuel metering/vehicle speed sensors and detonation sensors, altitude sensors, flow sensors, throttle position sensors, solenoids, stepper motors, actuators – fuel metering actuator, fuel injector, and ignition actuator.

UNIT–V: Electronic Vehicle Management System and Automotive Instrumentation System

Cruise control system, antilock braking system, electronic suspension system, electronic steering control, and transmission control, safety: air bags, collision avoidance radar warning system with block diagram, low tire pressure warning system, advanced cruise control system.

Speech synthesis, sensor multiplexing, control signal multiplexing with block diagram, fibre optics inside the car, automotive internal navigation system, GPS navigation system, voice recognition cell phone dialling.

Text Books

1. William B. Ribbens, "Understanding Automotive Electronics", SAMS/Elsevier Publishing, 6th Edition. (UNITS I -V).
2. Robert Bosch Gambh, "Automotive Electrics Automotive Electronics Systems and Components", John Wiley& Sons Ltd., 5th edition, 2007.

Reference Books

1. Ronald K Jurgen, "Automotive Electronics Handbook", 2nd Edition, McGraw-Hill, 1999.
2. G. Meyer, J. Valldorf and W. Gessner, "Advanced Microsystems for Automotive Applications", Springer, 2009.
3. Robert Bosch, "Automotive Hand Book" SAE, 5th Edition, 2000.

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Open Elective

SOFT COMPUTING TECHNIQUES

III Semester

Lecture	: 3	Internal Marks	: 30
Credits	: 3	External Marks	: 70

Course Objectives

- To develop the skills to gain a basic understanding of neural network theory and fuzzy logic theory.
- To introduce students to artificial neural networks and fuzzy theory from an engineering perspective

Course Outcomes

Upon successful completion of the course, the students will be able to

- comprehend the fuzzy logic and the concept of fuzziness involved in various systems and fuzzy set theory.
- understand the concepts of fuzzy sets, knowledge representation using fuzzy rules, approximate reasoning, fuzzy inference systems, and fuzzy logic
- understand the fundamental theory and concepts of neural networks, Identify different neural network architectures, algorithms, applications and their limitations
- understand appropriate learning rules for each of the architectures and learn several neural network paradigms and its applications
- reveal different applications of these models to solve engineering and other problems.

Course Content

UNIT–I: Fuzzy Set Theory

Introduction to Neuro – Fuzzy and Soft Computing, Fuzzy Sets, Basic Definition and Terminology, Set-theoretic Operations, Member Function Formulation and Parameterization, Fuzzy Rules and Fuzzy Reasoning, Extension Principle and Fuzzy Relations, Fuzzy If-Then Rules, Fuzzy Reasoning, Fuzzy Inference Systems, Mamdani Fuzzy Models, Surgeon Fuzzy Models, Tsukamoto Fuzzy Models, Input Space Partitioning and Fuzzy Modeling.

UNIT–II: Optimization

Derivative based Optimization, Descent Methods, The Method of Steepest Descent, Classical Newton's Method, Step Size Determination, Derivative-free Optimization, Genetic Algorithms, Simulated Annealing and Random Search – Downhill Simplex Search..

UNIT–III: Artificial Intelligence

Introduction, Knowledge Representation, Reasoning, Issues and Acquisition: Prepositional and Predicate Calculus Rule Based knowledge Representation Symbolic Reasoning under Uncertainty Basic knowledge Representation Issues Knowledge acquisition, Heuristic Search: Techniques for Heuristic search Heuristic Classification State Space Search: Strategies Implementation of Graph Search based on Recursion Patent directed Search Production System and Learning.

UNIT–IV: Neuro Fuzzy Modeling

Adaptive Neuro-Fuzzy Inference Systems, Architecture – Hybrid Learning Algorithm, Learning Methods that Cross-fertilize ANFIS and RBFN – Coactive Neuro Fuzzy Modeling, Framework Neuron Functions for Adaptive Networks – Neuro Fuzzy Spectrum.

UNIT–V: Applications of Computational Intelligence

Printed Character Recognition, Inverse Kinematics Problems, Automobile Fuel Efficiency Prediction, Soft Computing for Color Recipe Prediction.

Text Books

1. J.S.R.Jang, C.T.Sun and E.Mizutani, "Neuro-Fuzzy and Soft Computing", PHI, 2004, Pearson Education 2004.
2. N.P.Padhy, "Artificial Intelligence and Intelligent Systems", Oxford University Press, 2006.

Reference Books

1. Elaine Rich & Kevin Knight, Artificial Intelligence, Second Edition, Tata Mcgraw Hill Publishing Comp., 2006, New Delhi.
2. Timothy J.Ross, "Fuzzy Logic with Engineering Applications", McGraw-Hill, 1997.
3. Davis E.Goldberg, "Genetic Algorithms: Search, Optimization and Machine Learning", Addison Wesley, N.Y., 1989.

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